PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-150664
(43)Date of publication of application : 30.05.2000

(51)Int.Cl. H01L 21/8234
H01L 27/088
H01L 27/04
H01L 21/822
H01L 21/8238
H01L 27/092
H01L 29/78
H01L 29/786

(21)Application number : 10-324609
(22)Date of filing : 16.11.1998

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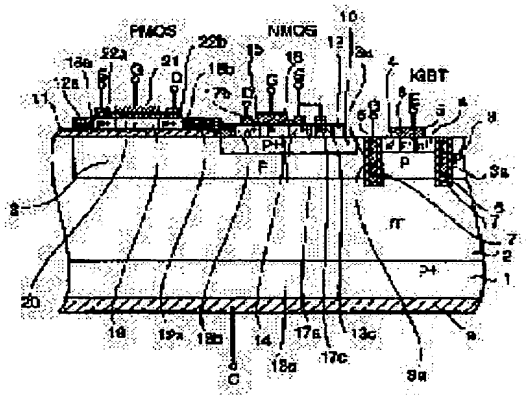
(54) HIGH BREAKDOWN STRENGTH SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a highly reliable high breakdown strength semiconductor device at a low cost in which a high breakdown strength element and a drive circuit or a protection circuit, etc., are formed integrally.
SOLUTION: This semiconductor device is provided with an n-type MOS semiconductor element which is provided with a source layer 13a, a drain layer 13b, a gate insulation film 15, and a gate electrode 15 formed on an epitaxial single crystal semiconductor layer 10 on the surface of a semiconductor substrate, a p-type second MOS semiconductor element which is provided with a source layer 18a, a drain layer 18b, a gate insulation film 20, and a gate electrode 21 formed on a polycrystalline semiconductor layer that is piled up on the semiconductor substrate with an insulation film 11 interposed, and a high breakdown strength semiconductor element such as an IGBT(insulated gate bipolar transistor), etc., formed on the semiconductor substrate.



LEGAL STATUS

[Date of request for examination] 02.11.2004
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate.
[Claim 2] The base layer of n mold with which said high proof-pressure semiconductor device was formed in said semi-conductor substrate, The 3rd source layer of n mold formed in the front face of the base layer of p mold formed in the front face of this n type of base layer, and this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, The 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, The high proof-pressure semiconductor device according to claim 1 characterized by having the 1st contact electrode which touches said 3rd source layer and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.
[Claim 3] Said 1st source layer and the 1st drain layer are a high proof-pressure semiconductor device according to claim 2 characterized by being formed in the front face of said p type of base layer.
[Claim 4] The high proof-pressure semiconductor device according to claim 3 characterized by forming the semi-conductor layer of high-concentration p mold rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.
[Claim 5] The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face at the epitaxial single crystal half conductor layer by which the laminating was carried out, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate.
[Claim 6] The base layer of n mold with which said high proof-pressure semiconductor device

was formed in said semi-conductor substrate, The 3rd source layer of n mold formed in the front face of the base layer of p mold formed in the front face of this n type of base layer, and this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, The 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, The high proof-pressure semiconductor device according to claim 5 characterized by having the 1st contact electrode which touches said 3rd source layer and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[Claim 7] Said epitaxial single crystal half conductor layer is a high proof-pressure semiconductor device according to claim 6 characterized by being formed in the front face of said p type of base layer.

[Claim 8] The high proof-pressure semiconductor device according to claim 7 characterized by forming the semi-conductor layer of high-concentration p mold rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.

[Claim 9] The 1st source layer and the 1st drain layer which the insulator layer was formed on the semi-conductor substrate, and were formed in the semi-conductor layer which grew epitaxially ranging from said semi-conductor substrate front face to said insulator layer top, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor layer front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the part on said insulator layer of said semi-conductor layer, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said semi-conductor layer front face between this 2nd source layer and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate.

[Claim 10] It is the high proof-pressure semiconductor device according to claim 9 characterized by forming the 1st source layer of said 1st MOS mold semiconductor device in the part of said semi-conductor substrate front face of said epitaxially grown semi-conductor layer, and forming the 1st drain layer of the component concerned in the part on said insulator layer of said semi-conductor layer, respectively.

[Claim 11] The base layer of n mold with which said high proof-pressure semiconductor device was formed in said semi-conductor substrate, The 3rd source layer of n mold formed in the front face of the base layer of p mold formed in the front face of this n type of base layer, and this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, The 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, The high proof-pressure semiconductor device according to claim 9 or 10 characterized by having the 1st contact electrode which touches said 3rd source layer and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[Claim 12] The part in which said 1st source layer of said epitaxially grown semi-conductor layer was formed is a high proof-pressure semiconductor device according to claim 11 characterized by being formed in the front face of said p type of base layer.

[Claim 13] The high proof-pressure semiconductor device according to claim 12 characterized by forming the semi-conductor layer of high-concentration p mold rather than the p type concerned of base layer between said 1st source layer and said p type of base layers.

[Claim 14] It is the high proof-pressure semiconductor device according to claim 9 to 13 characterized by for said epitaxially grown semi-conductor layer consisting of a single crystal, and the part on said insulator layer of said semi-conductor layer consisting of polycrystal.

[Claim 15] Said 3rd drain layer is a high proof-pressure semiconductor device claim 2 characterized by being p type layer 4 and 6 thru/or 8 or 11 thru/or given in 14.

[Claim 16] It is a high proof-pressure semiconductor device claim 2 characterized by for said high proof-pressure semiconductor device being a semiconductor device of a vertical mold, and forming said 3rd drain layer in the front face of said n type of the opposite side of base layer to

said 3rd source layer 4 and 6 8 and 11 thru/or given in 15.
[Claim 17] Claim 2 characterized by forming a slot so that it may pierce through said 3rd source layer and said p type of base layer and said n type of base layer may be reached, and embedding said 3rd gate electrode through said 3rd gate dielectric film into this slot 4 and 6 8 and 11 thru/or a high proof-pressure semiconductor device given in 16.
[Claim 18] Claim 2 characterized by forming the semi-conductor layer of high-concentration n mold rather than the n type concerned of base layer between said n type of base layer, and said 3rd drain layer 4 and 6 8 and 11 thru/or a high proof-pressure semiconductor device given in 17.

[Claim 19] Said n type of 1st MOS mold semiconductor device and said p type of 2nd MOS mold semiconductor device are a high proof-pressure semiconductor device according to claim 1 to 18 characterized by constituting a CMOS circuit.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the high proof-pressure vertical mold semiconductor device which has an MOS mold semiconductor device with respect to a high proof-pressure semiconductor device.
[0002]
[Description of the Prior Art] High proof-pressure components, such as IGBT (Insulated Gate Bipolar Transistor), are used in many industrial fields, such as motor control and a power source. In order that this high proof-pressure component may treat large power, many vertical mold components which use the front face and rear face of a silicon substrate as a cathode, an anode or an emitter, and a collector are used.
[0003] In order to make easy to use a high proof-pressure component, especially vertical mold components, such as such IGBT, a drive circuit and a protection network are made to unify, and being hard to break and high-performance-izing a high proof-pressure component is performed. Usually, such a circuit is made apart from the chip of high proof-pressure components, such as IGBT, and the gestalt of the module of carrying in the same package is taken.
[0004] Although it became advantageous by leaps and bounds in respect of cost and dependability when these circuits could be carried on the same chip, there was no means to attain this easily with the conventional technique. For example, since the carrier plasma exists in the interior of IGBT when made on the same chip, a drive circuit, a protection network, for example, a CMOS circuit etc., etc., there is a problem that n mold MOS transistor (it is hereafter called NMOS for short.) and p mold MOS transistor (it is hereafter called PMOS for short.) will carry out a latch rise simply.
[0005] Moreover, in order to solve the above-mentioned problem, a polish recon layer is formed through an insulator layer on IGBT prepared in the semi-conductor substrate, and there is a high proof-pressure semiconductor device which prepared the CMOS circuit in this polish recon layer. Drawing 6 is the sectional view showing the structure of this high proof-pressure semiconductor device.
[0006] As shown in drawing 6 , this high proof-pressure semiconductor device is a trench gate mold vertical mold quantity proof-pressure semiconductor device. n mold base layer 2 of high resistance is formed in the semi-conductor substrate, and high-concentration p mold drain layer 1 is formed in the whole surface of this n mold base layer 2. The drain electrode 9 is in contact with p mold drain layer 1. Moreover, p mold base layer 3 is formed in the field of another side of n mold base layer 2, and high-concentration n mold source layer 4 and high-concentration p mold contact layer 5 are formed in the front face of this p mold base layer 3.
[0007] Furthermore, two or more trench 3a is formed in the above-mentioned semi-conductor substrate front face. Such trench 3a is mutually arranged in parallel in the stripe-like top-face configuration (not shown), and it is formed so that n mold source layer 4 and p mold base layer 3 may be penetrated and n mold base layer 2 may be reached. In two or more trench 3a, the gate electrode 7 is embedded through gate dielectric film 6.
[0008] The above-mentioned n mold source layer 4 is formed in the field of the semi-conductor

substrate front face between two or more trench 3a in contact with gate dielectric film 6, and as it is surrounded by n mold source layer 4, p mold contact layer 5 is formed so that clearly [drawing 6]. Moreover, in contact with n mold source layer 4 and p mold contact layer 5, the source electrode 8 is in contact.

[0009] As mentioned above, the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0010] That is, on p mold base layer 3, the polycrystal (Pori) silicon layer 122 is formed through an insulator layer 121, NMOS and PMOS are formed in this polish recon layer 122, and NMOS and PMOS are further divided into each other by isolation insulator layer 122a.

[0011] NMOS consists of source electrode 105a and drain electrode 105b which contact source layer 101a formed in the polish recon layer 122 and drain layer 101b, the channel field 102 formed among these, the gate electrode 104 formed through the gate insulating layer 103 on this, source layer 101a, and drain layer 101b, respectively.

[0012] On the other hand, PMOS consists of source electrode 115a and drain electrode 115b which contact source layer 111a formed in the polish recon layer 122 and drain layer 111b, the channel field 112 formed among these, the gate electrode 114 formed through the gate insulating layer 113 on this, source layer 111a, and drain layer 111b, respectively.

[0013] IGBT and a CMOS circuit can be once carried on the same chip as mentioned above. However, the problem that a property is bad and cannot construct a highly precise analog circuit produces the CMOS semiconductor device formed in the polish recon layer prepared on the semi-conductor substrate.

[0014] That is, although a property with comparatively good PMOS formed in the polish recon layer is acquired, NMOS similarly formed in the polish recon layer has low channel mobility compared with NMOS formed in the single-crystal-silicon layer, and saturation characteristics are not acquired, either. Drawing 7 is the property Fig. showing the relation of the electrical potential difference between source drains of NMOS and PMOS (axis of abscissa) and drain current (axis of ordinate) which were formed in the polish recon layer. It turns out that drawing 7 (a) shows the property in the case of NMOS, a drain current also increases it by the increment in the electrical potential difference between source drains, and saturation characteristics are not acquired. On the other hand, although drawing 7 (b) shows the property in the case of PMOS and a drain current also increases it by the increment in the electrical potential difference between source drains, it turns out that saturation characteristics are acquired.

[0015]

[Problem(s) to be Solved by the Invention] the high proof-pressure component which was made to unify a drive circuit and a protection network in order to make a high proof-pressure component easy to use, could not break easily, and was high-performance-ized as stated above -- dependability -- although to provide by low cost highly was tried, there was no means to attain this easily with the conventional technique.

[0016] For example, since the carrier plasma exists in the interior of IGBT when made on the same chip, a drive circuit, a protection network, for example, a CMOS circuit etc., etc., there is a problem that NMOS and PMOS will carry out a latch rise simply.

[0017] Moreover, the problem that a property is bad and cannot construct a highly precise analog circuit produces the CMOS semiconductor device formed in the polish recon layer prepared on the semi-conductor substrate. the high proof-pressure semiconductor device which this invention was made in view of the above-mentioned actual condition, and unified the high proof-pressure component and the drive circuit, the protection network, etc. -- dependability -- it aims at providing by low cost highly.

[0018]

[Means for Solving the Problem] In order to solve the technical problem mentioned above, the 1st of this invention The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st

source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0019] Moreover, the 1st source layer and the 1st drain layer by which the 2nd of this invention was formed in the semi-conductor substrate front face at the epitaxial single crystal half conductor layer by which the laminating was carried out, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0020] Moreover, the 1st source layer and the 1st drain layer which, as for the 3rd of this invention, the insulator layer was formed on the semi-conductor substrate, and were formed in the semi-conductor layer which grew epitaxially ranging from said semi-conductor substrate front face to said insulator layer top, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor layer front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the part on said insulator layer of said semi-conductor layer, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said semi-conductor layer front face between this 2nd source layer and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.

[0021] In above-mentioned this invention, it is desirable to provide the following configurations. In the 1st of this invention, and 2 and 3 (1) Said high proof-pressure semiconductor device The base layer of n mold formed in said semi-conductor substrate, and the base layer of p mold formed in the front face of this n type of base layer, The 3rd source layer of n mold formed in the front face of this p type of base layer, and the contact layer of p mold, The 3rd gate electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, Have the 1st contact electrode which touches the 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, said 3rd source layer, and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[0022] (2) In the 1st of this invention, and 2 and 3, said 3rd drain layer should be p type layer. (3) Said high proof-pressure semiconductor device is a semiconductor device of a vertical mold, and said 3rd drain layer should be formed in the front face of said n type of the opposite side of base layer to said 3rd source layer in the 1st of this invention, and 2 and 3.

[0023] (4) A slot should be formed to pierce through said 3rd source layer and said p type of base layer, and to reach said n type of base layer, and said 3rd gate electrode should be embedded through said 3rd gate dielectric film in the 1st of this invention, and 2 and 3 in this slot.

[0024] (5) In the 1st of this invention, and 2 and 3, the semi-conductor layer of high-concentration n mold should be formed rather than the n type concerned of base layer between said n type of base layer, and said 3rd drain layer.

[0025] (6) this invention -- the -- one -- two -- three -- setting -- said -- n -- a mold -- the

-- one -- MOS -- a mold -- a semiconductor device -- said -- p -- a mold -- the -- two -- MOS -- a mold -- a semiconductor device -- a CMOS circuit -- constituting -- things -- (-- seven --) -- this invention -- the -- one -- setting -- said -- the -- one -- the source -- a layer -- and -- the -- one -- a drain -- a layer -- said -- p -- a mold -- the base -- a layer -- a front face -- forming -- having -- **** .

[0026] (8) In the 2nd of this invention, said epitaxial single crystal half conductor layer should be formed in the front face of said p type of base layer.

(9) In the 1st of this invention, and 2, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.

[0027] (10) In the 3rd of this invention, the 1st source layer of said 1st MOS mold semiconductor device should be formed in the part of said semi-conductor substrate front face of said epitaxially grown semi-conductor layer, and the 1st drain layer of the component concerned should be formed in the part on said insulator layer of said semi-conductor layer, respectively.

[0028] (11) In the 3rd of this invention, the part in which said 1st source layer of said epitaxially grown semi-conductor layer was formed should be formed in the front face of said p type of base layer.

[0029] (12) In the 3rd of this invention, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and said p type of base layers.

[0030] (13) In the 3rd of this invention, said epitaxially grown semi-conductor layer should consist of a single crystal, and the part on said insulator layer of said semi-conductor layer should consist of polycrystal. In this invention, NMOS is formed in the epitaxial crystal layer prepared on the same silicon substrate as high proof-pressure semiconductor devices, such as IGBT, or this, for example, and PMOS is prepared on the polish recon layer prepared on the oxide film.

[0031] Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. According to this invention, since IGBT etc. has p base diffusion layer, it can form NMOS comparatively easily into this p base diffusion layer like especially the 1st of this invention. According to this configuration, it is possible to acquire a good NMOS property.

[0032] Since leakage current may become large with this configuration for the plasma which exists in the interior, such as IGBT, the configuration shown below is more desirable. That is, it is desirable to prepare a short electrode between p bases and the sources concerned so that p base potential of NMOS may become the same as the source potential of high proof-pressure semiconductor devices, such as IGBT.

[0033] Moreover, in the 2nd of this invention, and the 3rd, it is possible to use the approach of preparing a silicon oxide pattern on a silicon substrate, applying on this silicon oxide pattern from on p base, preparing an amorphous silicon layer for example, annealing this at about 600 degrees C, and crystallizing. By this approach, an epitaxial growth silicon layer is formed on the above-mentioned p base, NMOS can be produced in this layer, and a polish recon layer is formed on the above-mentioned silicon oxide pattern, and PMOS can be produced in this layer. Consequently, PMOS formed in this polish recon layer and NMOS formed in the epitaxial growth silicon layer become possible [acquiring a good property also for ** in channel mobility and saturation characteristics].

[0034] A part of amorphous silicon layer made to extend on the above-mentioned silicon oxide pattern further again can also be considered as the epitaxial growth phase of a single crystal in the part near the above-mentioned p base. Therefore, it is possible to form the drain of NMOS, a channel (base), or the source in this part. For example, a channel (base) is formed in the single crystal epitaxial growth phase on a silicon oxide pattern, and the source of NMOS forms a drain in the epitaxial growth phase on p base at the epitaxial growth phase on the oxide-film pattern concerned (a single crystal or polish recon).

[0035] According to this configuration, a good property can be acquired in channel mobility and saturation characteristics, and increase of leakage current can be prevented. Furthermore, since a drain exists on a silicon oxide pattern, it is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by p mold drain layer of IGBT prepared in the silicon substrate, the high resistance n type layer, p mold base layer, and n mold source layer of NMOS.
[0036] As mentioned above, if this invention is caused, since NMOS will be prepared in a semi-conductor substrate or the epitaxial growth phase on it and PMOS will be prepared in the polycrystal layer on an insulator layer, good NMOS and a PMOS property can be acquired and it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with high proof-pressure semiconductor devices, such as IGBT.
[0037]
[Embodiment of the Invention] It explains to a detail, using a drawing hereafter about the operation gestalt concerning the high proof-pressure semiconductor device of this invention.
(1st operation gestalt) Drawing 1 is the sectional view showing the high proof-pressure semiconductor device concerning the 1st operation gestalt of this invention. The high proof-pressure semiconductor device of this operation gestalt is the trench gate mold vertical mold IGBT.
[0038] as shown in drawing 1 , n mold base layer 2 of high resistance forms in a semi-conductor substrate (silicon substrate) -- having -- **** -- p+ of high concentration [whole surface / of this n mold base layer 2] The mold drain layer 1 is formed. The drain electrode 9 is in contact with p mold drain layer 1. moreover, p mold base layer 3 forms in the field of another side of n mold base layer 2 -- having -- **** -- n+ of high concentration [front face / of this p mold base layer 3] The mold source layer 4 and high-concentration p+ The mold contact layer 5 is formed.
[0039] Furthermore, two or more trench 3a is formed in the above-mentioned semi-conductor substrate front face. It is mutually arranged in parallel in the stripe-like top-face configuration (not shown), and such trench 3a is n+. It is formed so that the mold source layer 4 and p mold base layer 3 may be penetrated and n mold base layer 2 may be reached. In two or more trench 3a, the gate electrode 7 is embedded through gate dielectric film 6.
[0040] In the field of the semi-conductor substrate front face between two or more trench 3a, it is above-mentioned n+ so that clearly [drawing 1]. The mold source layer 4 is formed in contact with gate dielectric film 6, and it is n+. It is p+ as it is surrounded by the mold source layer 4. The mold contact layer 5 is formed. Moreover, n+ mold source layer 4 and p+ In contact with the mold contact layer 5, the source electrode 8 is in contact. p+ Two or more arrangement may be carried out among trench 3a, and the mold contact layer 5 is n+. The mold source layer 4 and p+ It is the n+ concerned in order to take certainly contact of the source electrode 8 to the mold contact layer 5. The mold source layer 4 and p+ As for the mold contact layer 5, it is desirable to be arranged by turns along with the longitudinal direction of trench 1a.
[0041] As mentioned above, the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.
[0042] Namely, p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] The mold diffusion layer 10 is formed and it is this p+. The epitaxial single-crystal-silicon layer 12 is formed on the mold diffusion layer 10. On the other hand, it is p+. The insulating-layer pattern 11 is formed in a different field from the mold diffusion layer 10, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12a.
[0043] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 13a and drain layer 13b of a mold, The channel field 14 formed among these, the gate electrode

16 formed through the gate insulating layer 15 on this, and p+ adjoined and formed in source layer 13a Contact layer 13c of a mold, It consists of source layer 13a, drain layer 13b and source electrode 17a that contacts contact layer 13c, respectively, drain electrode 17b, and contact electrode 17c. Source electrode 17a and contact electrode 17c are electrically connected to each other.

[0044] On the other hand, PMOS is n+ formed in the polish recon layer. It consists of source electrode 22a and drain electrode 22b which contact source layer 18a of a mold and drain layer 18b, the channel field 19 formed among these, the gate electrode 21 formed through the gate insulating layer 20 on this, source layer 18a, and drain layer 18b, respectively.

[0045] As mentioned above, in this operation gestalt, while forming the epitaxial single-crystal-silicon layer 12 on the silicon substrate in which IGBT was formed and forming NMOS in this crystal layer 12, PMOS is prepared on the polish recon layer formed on the oxide film 11. Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. However, according to this operation gestalt, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics, and increase of leakage current can be prevented.

[0046] Moreover, since NMOS is formed in the amorphous silicon layer 10 crystallized on p mold base layer 3, a threshold becomes proper. That is, although the surface concentration of p mold base layer of the usual IGBT may be too high for NMOS, if the amorphous silicon layer which is not doped is formed on p mold base layer, even if p mold impurity is spread in the crystallization amorphous silicon layer 10 from p mold base layer, the surface concentration of the p mold base layer concerned will become lower than that of p mold base layer of IGBT, and the threshold of NMOS will be rationalized.

[0047] It is p+ further again. p mold drain layer 1 of IGBT prepared in the silicon substrate since the mold diffusion layer 10 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 13a of a mold or drain layer 13b.

[0048] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0049] The manufacture approach of the high proof-pressure semiconductor device by this operation gestalt described above is as stating below. first, trench 1a of a vertical mold IGBT -- forming -- preceding -- the front face of p mold base layer 3 of a semi-conductor substrate -- p+ the mold diffusion layer 10 -- forming -- this p+ the field except the mold diffusion layer 10 and an IGBT formation schedule field -- alternative -- an oxide film 11 -- for example, LOCOS -- it forms by law. After forming an oxide film 11, this oxide-film 11 grade is used as a mask here, and it is p+ by an ion implantation etc. The mold diffusion layer 10 may be formed.

[0050] Next, p+ of p mold base layer 3 front face Apply on an oxide film 11 from the mold diffusion layer 10, and about 0.5 micrometers of amorphous silicon (a-Si) layers are made to deposit, at 600 degrees C, it anneals for about 20 hours and solid phase growth is carried out. It is p+ by this annealing. While single-crystal-izing the amorphous silicon layer on the mold diffusion layer 10 and becoming the epitaxial single-crystal-silicon layer 12, the amorphous silicon layer on an oxide film 11 turns into a polish recon layer.

[0051] Then, by the ion implantation, n mold impurity is introduced into the field to which PMOS of said polish recon layer is formed in the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed in p mold impurity, respectively, and it considers as the p type semiconductor layer 14 and the n-type-semiconductor layer 19, respectively. Furthermore, isolation oxide-film 12a which divides these components into an oxidation part is formed by oxidizing the field except the field in which PMOS of the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed, and said polish recon layer is formed.

[0052] Next, in order to form the gate of IGBT, trench 3a is formed in a silicon substrate. The gate oxide (15 20) of NMOS and PMOS is formed [the inside of trench 3a] in the front face of

the epitaxial single-crystal-silicon layer 12 and the above-mentioned polish recon layer for gate oxide 6 at coincidence, respectively. Furthermore, the polish recon film is deposited so that a trench may be embedded on this, and the gate electrode 7 of IGBT is produced. This polish recon film is deposited also on the gate oxide (15 20) of NMOS and PMOS at coincidence, and can also form the gate electrode (16 21) of NMOS and PMOS.

[0053] next, the gate electrode 7 and a gate electrode (16 21) -- a mask -- carrying out -- respectively -- an ion implantation -- n+ of IGBT n+ of the mold source layer 4 and NMOS mold source layer 13a and the drain layer 13 -- p+ of b and PMOS Mold source layer 18a and drain layer 18b are formed. Moreover, p+ of IGBT p+ of the mold contact layer 5 and NMOS Mold contact layer 13c is formed by the ion implantation.

[0054] Then, n+ of IGBT The mold source layer 4 and p+ The drain electrode 9 is formed in the source electrode 8 and p mold drain layer 1 at the mold contact layer 5. To source layer 13a of NMOS, drain layer 13b, and contact layer 13c, respectively Source electrode 17a, Drain electrode 17b and contact electrode 17c are formed, source electrode 22a and drain electrode 22b are formed in source layer 18a of PMOS, and drain layer 18b, respectively, and the high proof-pressure semiconductor device of this operation gestalt is completed.

[0055] (2nd operation gestalt) Drawing 2 is the sectional view showing the high proof-pressure semiconductor device concerning the 2nd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1 , and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that a part of epitaxial single-crystal-silicon layer is formed on an insulating-layer pattern, and the drain layer of NMOS and a part of channel field are formed in a part of this single-crystal-silicon layer.

[0056] As shown in drawing 2 , the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0057] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, the polycrystal (Pori) silicon layer is prepared on the insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12b.

[0058] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 31a and drain layer 31b of a mold, The channel field 32 formed among these, the gate electrode 34 formed through the gate insulating layer 33 on this, and p+ adjoined and formed in source layer 31a Contact layer 31c of a mold, It consists of drain electrode 35b in contact with source electrode 35a in contact with source layer 31a and contact layer 31c, and drain layer 31b. A part of drain layer 31b of NMOS and channel field 32 are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and source layer 31a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0059] On the other hand, PMOS is n+ formed in the polish recon layer. It consists of source electrode 45a and drain electrode 45b which contact source layer 41a of a mold and drain layer 41b, the channel field 42 formed among these, the gate electrode 44 formed through the gate insulating layer 43 on this, source layer 41a, and drain layer 41b, respectively.

[0060] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0061] Also in this operation gestalt, like the 1st operation gestalt, it applies on the insulating-layer pattern 11 from p mold base layer 3 of a silicon substrate, and an amorphous silicon layer is formed, and this amorphous silicon layer is single-crystal-ized, using a silicon substrate as seed crystal. By this single crystal-ization, a part of part near seed crystal also single-crystal-izes the amorphous silicon layer on the insulating-layer pattern 11. By forming a part of channel

field 32 of NMOS, and drain layer 31b in the part of this single-crystal-ized amorphous silicon layer, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 31b for the channel field 32 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case.

[0062] p mold drain layer 1 of IGBT prepared in the silicon substrate further again since the insulating-layer pattern 11 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 31b of a mold.

[0063] in addition, the 1st operation gestalt -- the same -- p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms -- having -- this p+ The channel field 32, source layer 31a, and contact layer 31c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 31a of a mold.

[0064] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0065] (3rd operation gestalt) Drawing 3 is the sectional view showing the high proof-pressure semiconductor device concerning the 3rd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 2 , and detailed explanation is omitted. The point that this operation gestalt differs from the 2nd operation gestalt is a point that the drain layer of NMOS, all of channel fields, and a part of source layer are formed in a part of epitaxial single-crystal-silicon layer formed on the insulating-layer pattern.

[0066] As shown in drawing 3 , the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0067] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, on the insulating-layer pattern 11, 12f of polycrystal (Pori) silicon layers is prepared. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS (not shown) is formed in 12f of polish recon layers on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12c.

[0068] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 51a and drain layer 51b of a mold, The channel field 52 formed among these, the gate electrode 54 formed through the gate insulating layer 53 on this, and p+ adjoined and formed in source layer 51a Contact layer 51c of a mold, It consists of drain electrode 55b in contact with source electrode 55a in contact with source layer 51a and contact layer 51c, and drain layer 51b. A part for drain layer 51b of NMOS and all of the channel fields 52 and a part of source layer 51a are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and a part of source layer 51a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0069] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0070] Also in this operation gestalt, the amorphous silicon layer formed on the insulating-layer

pattern 11 from p mold base layer 3 of a silicon substrate, having applied is single-crystal-ized like the 2nd operation gestalt, using a silicon substrate as seed crystal. When a part of part also with the amorphous silicon layer near seed crystal on the insulating-layer pattern 11 single-crystal-izes and forms a part for drain layer 51b of NMOS, and all of the channel fields 52, and a part of source layer 51a in the part of this single-crystal-ized amorphous silicon layer by this single crystal-ization, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 51b for the channel field 52 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case. Moreover, since the channel field 52 of NMOS is completely insulated from the silicon substrate with this structure, as for this channel field 52, it is hard to be influenced of the potential of a silicon substrate, and a setup of a threshold and control become easy.

[0071] p mold drain layer 1 of IGBT prepared in the silicon substrate with the insulating-layer pattern 11 further again, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 51b of a mold.

[0072] in addition, the 1st operation gestalt -- the same -- p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms -- having -- this p+ Source layer 51a and contact layer 51c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 51a of a mold.

[0073] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0074] (4th operation gestalt) Drawing 4 is the sectional view showing the high proof-pressure semiconductor device concerning the 4th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1 , and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that NMOS is formed in p mold base layer of IGBT of a silicon substrate, and high-concentration p type layer is formed between this NMOS and p mold base layer.

[0075] As shown in drawing 4 , the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0076] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and 12g of polycrystal (Pori) silicon layers is prepared on this insulating-layer pattern 11. PMOS is formed in 12g of this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and PMOS are divided into each other by 12d of isolation insulator layers.

[0077] That is, NMOS is n+ formed in p type semiconductor layer 3b. Source layer 61a and drain layer 61b of a mold, The channel field 62 formed among these, the gate electrode 64 formed through the gate insulating layer 63 on this, and p+ adjoined and formed in source layer 61a Contact layer 61c of a mold, It consists of drain electrode 65b in contact with source electrode 65a in contact with source layer 61a and contact layer 61c, and drain layer 61b. p+ of high concentration [b / under Above NMOS / p type semiconductor layer 3/ layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.

[0078] On the other hand, PMOS is n+ formed in 12g of polish recon layers. It consists of source electrode 75a and drain electrode 75b which contact source layer 71a of a mold and drain layer

71b, the channel field 72 formed among these, the gate electrode 74 formed through the gate insulating layer 73 on this, source layer 71a, and drain layer 71b, respectively.
[0079] According to this operation gestalt, since NMOS is formed in p type semiconductor layer 3b of a silicon substrate, NMOS will be formed in the crystalline good single crystal part, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics like the 1st operation gestalt, and increase of leakage current can be prevented.
[0080] Moreover, since NMOS is formed in the low-concentration p type semiconductor layer 3 rather than p mold base layer 3 of IGBT, it is also possible to rationalize the threshold of the NMOS concerned. Formation of this p type semiconductor layer 3 is performed in advance of formation of p mold base layer of IGBT.
[0081] p+ of high concentration [layer / 3 / p type semiconductor layer 3b or / p mold base] further again p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 61a of a mold or drain layer 61b.
[0082] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.
[0083] (5th operation gestalt) Drawing 5 is the sectional view showing the high proof-pressure semiconductor device concerning the 5th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 4 , and detailed explanation is omitted. The point that this operation gestalt differs from the 4th operation gestalt is a point that diode is formed in the polycrystal (Pori) silicon layer formed on the insulating-layer pattern.
[0084] As shown in drawing 5 , the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the diode described below is formed on the same chip as this high proof-pressure semiconductor device.
[0085] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. Diode is formed in this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and diode are divided into each other by isolation insulator layer 12e.
[0086] That is, NMOS is n+ formed in p type semiconductor layer 3b. Source layer 81a and drain layer 81b of a mold, The channel field 82 formed among these, the gate electrode 84 formed through the gate insulating layer 83 on this, and p+ adjoined and formed in source layer 81a Contact layer 81c of a mold, It consists of drain electrode 85b in contact with source electrode 85a in contact with source layer 81a and contact layer 81c, and drain layer 81b. p+ of high concentration [b / under Above NMOS / p type semiconductor layer 3/ layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.
[0087] On the other hand, diode is p+ formed in the polish recon layer. Anode layer 91a of a mold, and n+ It consists of anode electrode 92a and cathode electrode 92b which contact cathode layer 91b of a mold, anode layer 91a, and cathode layer 91b, respectively.
[0088] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS can be obtained like the 4th operation gestalt, and increase of leakage current can be prevented.
[0089] Moreover, it is also possible to rationalize the threshold of NMOS by the p type semiconductor layer 3 like the 4th operation gestalt. Furthermore, p+ p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 81a of a mold or drain layer 81b.
[0090] Thus, according to this operation gestalt, since a good NMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0091] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, p+ Between the mold drain layer 1 and n mold base layer 2, high-concentration n mold buffer layer can be formed rather than the n mold base layer 2 concerned, and it is possible to raise conductivity.
[0092] Moreover, although the above-mentioned operation gestalt explained the high proof-pressure semiconductor device of a vertical mold, this invention is applicable also to the high proof-pressure semiconductor device of a horizontal type. In this case, a drain layer is formed in the semi-conductor substrate front face of the same side as a source layer.
[0093] At the above-mentioned operation gestalt, it is p+ further again. It is a drain layer, although IGBT which has the drain layer of a mold was mentioned as the example and explained n+ It is also possible to consider as a mold and to apply to various quantity proof-pressure semiconductor devices, such as an MOS mold quantity proof-pressure semiconductor device and other thyristors. In addition, it is possible to deform variously and to carry out in the range which does not deviate from the meaning of this invention.
[0094]
[Effect of the Invention] the high proof-pressure semiconductor device which unified the high proof-pressure component and the drive circuit, the protection network, etc. according to this invention -- dependability -- it can provide by low cost highly.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] the high proof-pressure component which was made to unify a drive circuit and a protection network in order to make a high proof-pressure component easy to use, could not break easily, and was high-performance-ized as stated above -- dependability -- although to provide by low cost highly was tried, there was no means to attain this easily with the conventional technique.
[0016] For example, since the carrier plasma exists in the interior of IGBT when made on the same chip, a drive circuit, a protection network, for example, a CMOS circuit etc., etc., there is a problem that NMOS and PMOS will carry out a latch rise simply.
[0017] Moreover, the problem that a property is bad and cannot construct a highly precise analog circuit produces the CMOS semiconductor device formed in the polish recon layer prepared on the semi-conductor substrate. the high proof-pressure semiconductor device which this invention was made in view of the above-mentioned actual condition, and unified the high proof-pressure component and the drive circuit, the protection network, etc. -- dependability -- it aims at providing by low cost highly.

[Translation done.]

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MEANS

[Means for Solving the Problem] In order to solve the technical problem mentioned above, the 1st of this invention The 1st source layer and the 1st drain layer which were formed in the semi-conductor substrate front face, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.
[0019] Moreover, the 1st source layer and the 1st drain layer by which the 2nd of this invention was formed in the semi-conductor substrate front face at the epitaxial single crystal half conductor layer by which the laminating was carried out, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor substrate front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the polycrystal semi-conductor layer by which the laminating was carried out through the insulator layer on said semi-conductor substrate, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said polycrystal semi-conductor layer front face between the 2nd source layer concerned and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.
[0020] Moreover, the 1st source layer and the 1st drain layer which, as for the 3rd of this invention, the insulator layer was formed on the semi-conductor substrate, and were formed in the semi-conductor layer which grew epitaxially ranging from said semi-conductor substrate front face to said insulator layer top, The 1st MOS mold semiconductor device of n mold which has the 1st gate electrode formed in said semi-conductor layer front face between the 1st source layer concerned and the 1st drain layer through the 1st gate dielectric film, The 2nd source layer and the 2nd drain layer which were formed in the part on said insulator layer of said semi-conductor layer, The 2nd MOS mold semiconductor device of p mold which has the 2nd gate electrode formed in said semi-conductor layer front face between this 2nd source layer and the 2nd drain layer through the 2nd gate dielectric film, The high proof-pressure semiconductor device characterized by providing the high proof-pressure semiconductor device formed in said semi-conductor substrate is offered.
[0021] In above-mentioned this invention, it is desirable to provide the following configurations. In the 1st of this invention, and 2 and 3 (1) Said high proof-pressure semiconductor device The base layer of n mold formed in said semi-conductor substrate, and the base layer of p mold formed in the front face of this n type of base layer, The 3rd source layer of n mold formed in the front face of this p type of base layer, and the contact layer of p mold, The 3rd gate

electrode formed in the front face of said p type of base layer through the 3rd gate dielectric film, Have the 1st contact electrode which touches the 3rd drain layer formed in the location distant from said p type of base layer among the front faces of said n type of base layer, said 3rd source layer, and said p type of contact layer, and the 2nd contact electrode which touches said 3rd drain layer.

[0022] (2) In the 1st of this invention, and 2 and 3, said 3rd drain layer should be p type layer.

(3) Said high proof-pressure semiconductor device is a semiconductor device of a vertical mold, and said 3rd drain layer should be formed in the front face of said n type of the opposite side of base layer to said 3rd source layer in the 1st of this invention, and 2 and 3.

[0023] (4) A slot should be formed to pierce through said 3rd source layer and said p type of base layer, and to reach said n type of base layer, and said 3rd gate electrode should be embedded through said 3rd gate dielectric film in the 1st of this invention, and 2 and 3 in this slot.

[0024] (5) In the 1st of this invention, and 2 and 3, the semi-conductor layer of high-concentration n mold should be formed rather than the n type concerned of base layer between said n type of base layer, and said 3rd drain layer.

[0025] (6) this invention -- the -- one -- two -- three -- setting -- said -- n -- a mold -- the -- one -- MOS -- a mold -- a semiconductor device -- said -- p -- a mold -- the -- two -- MOS -- a mold -- a semiconductor device -- a CMOS circuit -- constituting -- things -- (-- seven --) -- this invention -- the -- one -- setting -- said -- the -- one -- the source -- a layer -- and -- the -- one -- a drain -- a layer -- said -- p -- a mold -- the base -- a layer -- a front face -- forming -- having -- **** .

[0026] (8) In the 2nd of this invention, said epitaxial single crystal half conductor layer should be formed in the front face of said p type of base layer.

(9) In the 1st of this invention, and 2, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and the 1st drain layer, and said p type of base layer.

[0027] (10) In the 3rd of this invention, the 1st source layer of said 1st MOS mold semiconductor device should be formed in the part of said semi-conductor substrate front face of said epitaxially grown semi-conductor layer, and the 1st drain layer of the component concerned should be formed in the part on said insulator layer of said semi-conductor layer, respectively.

[0028] (11) In the 3rd of this invention, the part in which said 1st source layer of said epitaxially grown semi-conductor layer was formed should be formed in the front face of said p type of base layer.

[0029] (12) In the 3rd of this invention, the semi-conductor layer of high-concentration p mold should be formed rather than the p type concerned of base layer between said 1st source layer and said p type of base layers.

[0030] (13) In the 3rd of this invention, said epitaxially grown semi-conductor layer should consist of a single crystal, and the part on said insulator layer of said semi-conductor layer should consist of polycrystal. In this invention, NMOS is formed in the epitaxial crystal layer prepared on the same silicon substrate as high proof-pressure semiconductor devices, such as IGBT, or this, for example, and PMOS is prepared on the polish recon layer prepared on the oxide film.

[0031] Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. According to this invention, since IGBT etc. has p base diffusion layer, it can form NMOS comparatively easily into this p base diffusion layer like especially the 1st of this invention. According to this configuration, it is possible to acquire a good NMOS property.

[0032] Since leakage current may become large with this configuration for the plasma which exists in the interior, such as IGBT, the configuration shown below is more desirable. That is, it is desirable to prepare a short electrode between p bases and the sources concerned so that p base potential of NMOS may become the same as the source potential of high proof-pressure

semiconductor devices, such as IGBT.
[0033] Moreover, in the 2nd of this invention, and the 3rd, it is possible to use the approach of preparing a silicon oxide pattern on a silicon substrate, applying on this silicon oxide pattern from on p base, preparing an amorphous silicon layer for example, annealing this at about 600 degrees C, and crystallizing. By this approach, an epitaxial growth silicon layer is formed on the above-mentioned p base, NMOS can be produced in this layer, and a polish recon layer is formed on the above-mentioned silicon oxide pattern, and PMOS can be produced in this layer. Consequently, PMOS formed in this polish recon layer and NMOS formed in the epitaxial growth silicon layer become possible [acquiring a good property also for ** in channel mobility and saturation characteristics].
[0034] A part of amorphous silicon layer made to extend on the above-mentioned silicon oxide pattern further again can also be considered as the epitaxial growth phase of a single crystal in the part near the above-mentioned p base. Therefore, it is possible to form the drain of NMOS, a channel (base), or the source in this part. For example, a channel (base) is formed in the single crystal epitaxial growth phase on a silicon oxide pattern, and the source of NMOS forms a drain in the epitaxial growth phase on p base at the epitaxial growth phase on the oxide-film pattern concerned (a single crystal or polish recon).
[0035] According to this configuration, a good property can be acquired in channel mobility and saturation characteristics, and increase of leakage current can be prevented. Furthermore, since a drain exists on a silicon oxide pattern, it is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by p mold drain layer of IGBT prepared in the silicon substrate, the high resistance n type layer, p mold base layer, and n mold source layer of NMOS.
[0036] As mentioned above, if this invention is caused, since NMOS will be prepared in a semi-conductor substrate or the epitaxial growth phase on it and PMOS will be prepared in the polycrystal layer on an insulator layer, good NMOS and a PMOS property can be acquired and it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with high proof-pressure semiconductor devices, such as IGBT.
[0037]
[Embodiment of the Invention] It explains to a detail, using a drawing hereafter about the operation gestalt concerning the high proof-pressure semiconductor device of this invention.
(1st operation gestalt) Drawing 1 is the sectional view showing the high proof-pressure semiconductor device concerning the 1st operation gestalt of this invention. The high proof-pressure semiconductor device of this operation gestalt is the trench gate mold vertical mold IGBT.
[0038] as shown in drawing 1 , n mold base layer 2 of high resistance forms in a semi-conductor substrate (silicon substrate) -- having -- **** -- p+ of high concentration [whole surface / of this n mold base layer 2] The mold drain layer 1 is formed. The drain electrode 9 is in contact with p mold drain layer 1. moreover, p mold base layer 3 forms in the field of another side of n mold base layer 2 -- having -- **** -- n+ of high concentration [front face / of this p mold base layer 3] The mold source layer 4 and high-concentration p+ The mold contact layer 5 is formed.
[0039] Furthermore, two or more trench 3a is formed in the above-mentioned semi-conductor substrate front face. It is mutually arranged in parallel in the stripe-like top-face configuration (not shown), and such trench 3a is n+. It is formed so that the mold source layer 4 and p mold base layer 3 may be penetrated and n mold base layer 2 may be reached. In two or more trench 3a, the gate electrode 7 is embedded through gate dielectric film 6.
[0040] In the field of the semi-conductor substrate front face between two or more trench 3a, it is above-mentioned n+ so that clearly [drawing 1]. The mold source layer 4 is formed in contact with gate dielectric film 6, and it is n+. It is p+ as it is surrounded by the mold source layer 4. The mold contact layer 5 is formed. Moreover, n+ mold source layer 4 and p+ In contact with the mold contact layer 5, the source electrode 8 is in contact. p+ Two or more arrangement may be carried out among trench 3a, and the mold contact layer 5 is n+. The mold source layer 4

and p+ It is the n+ concerned in order to take certainly contact of the source electrode 8 to the mold contact layer 5. The mold source layer 4 and p+ As for the mold contact layer 5, it is desirable to be arranged by turns along with the longitudinal direction of trench 1a.

[0041] As mentioned above, the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0042] Namely, p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] The mold diffusion layer 10 is formed and it is this p+. The epitaxial single-crystal-silicon layer 12 is formed on the mold diffusion layer 10. On the other hand, it is p+. The insulating-layer pattern 11 is formed in a different field from the mold diffusion layer 10, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12a.

[0043] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 13a and drain layer 13b of a mold, The channel field 14 formed among these, the gate electrode 16 formed through the gate insulating layer 15 on this, and p+ adjoined and formed in source layer 13a Contact layer 13c of a mold, It consists of source layer 13a, drain layer 13b and source electrode 17a that contacts contact layer 13c, respectively, drain electrode 17b, and contact electrode 17c. Source electrode 17a and contact electrode 17c are electrically connected to each other.

[0044] On the other hand, PMOS is n+ formed in the polish recon layer. It consists of source electrode 22a and drain electrode 22b which contact source layer 18a of a mold and drain layer 18b, the channel field 19 formed among these, the gate electrode 21 formed through the gate insulating layer 20 on this, source layer 18a, and drain layer 18b, respectively.

[0045] As mentioned above, in this operation gestalt, while forming the epitaxial single-crystal-silicon layer 12 on the silicon substrate in which IGBT was formed and forming NMOS in this crystal layer 12, PMOS is prepared on the polish recon layer formed on the oxide film 11. Although a property with comparatively good PMOS formed in the polish recon layer is acquired, when NMOS is formed in a polish recon layer, compared with what was formed in single crystal silicon, channel mobility is low, and saturation characteristics are not acquired, either. However, according to this operation gestalt, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics, and increase of leakage current can be prevented.

[0046] Moreover, since NMOS is formed in the amorphous silicon layer 10 crystallized on p mold base layer 3, a threshold becomes proper. That is, although the surface concentration of p mold base layer of the usual IGBT may be too high for NMOS, if the amorphous silicon layer which is not doped is formed on p mold base layer, even if p mold impurity is spread in the crystallization amorphous silicon layer 10 from p mold base layer, the surface concentration of the p mold base layer concerned will become lower than that of p mold base layer of IGBT, and the threshold of NMOS will be rationalized.

[0047] It is p+ further again. p mold drain layer 1 of IGBT prepared in the silicon substrate since the mold diffusion layer 10 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 13a of a mold or drain layer 13b.

[0048] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0049] The manufacture approach of the high proof-pressure semiconductor device by this operation gestalt described above is as stating below. first, trench 1a of a vertical mold IGBT -- forming -- preceding -- the front face of p mold base layer 3 of a semi-conductor substrate -- p+ the mold diffusion layer 10 -- forming -- this p+ the field except the mold diffusion layer 10 and an IGBT formation schedule field -- alternative -- an oxide film 11 -- for example, LOCOS

-- it forms by law. After forming an oxide film 11, this oxide-film 11 grade is used as a mask here, and it is p+ by an ion implantation etc. The mold diffusion layer 10 may be formed.
[0050] Next, p+ of p mold base layer 3 front face Apply on an oxide film 11 from the mold diffusion layer 10, and about 0.5 micrometers of amorphous silicon (a-Si) layers are made to deposit, at 600 degrees C, it anneals for about 20 hours and solid phase growth is carried out. It is p+ by this annealing. While single-crystal-izing the amorphous silicon layer on the mold diffusion layer 10 and becoming the epitaxial single-crystal-silicon layer 12, the amorphous silicon layer on an oxide film 11 turns into a polish recon layer.
[0051] Then, by the ion implantation, n mold impurity is introduced into the field to which PMOS of said polish recon layer is formed in the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed in p mold impurity, respectively, and it considers as the p type semiconductor layer 14 and the n-type-semiconductor layer 19, respectively. Furthermore, isolation oxide-film 12a which divides these components into an oxidation part is formed by oxidizing the field except the field in which PMOS of the field in which NMOS of the epitaxial single-crystal-silicon layer 12 is formed, and said polish recon layer is formed.
[0052] Next, in order to form the gate of IGBT, trench 3a is formed in a silicon substrate. The gate oxide (15 20) of NMOS and PMOS is formed [the inside of trench 3a] in the front face of the epitaxial single-crystal-silicon layer 12 and the above-mentioned polish recon layer for gate oxide 6 at coincidence, respectively. Furthermore, the polish recon film is deposited so that a trench may be embedded on this, and the gate electrode 7 of IGBT is produced. This polish recon film is deposited also on the gate oxide (15 20) of NMOS and PMOS at coincidence, and can also form the gate electrode (16 21) of NMOS and PMOS.
[0053] next, the gate electrode 7 and a gate electrode (16 21) -- a mask -- carrying out -- respectively -- an ion implantation -- n+ of IGBT n+ of the mold source layer 4 and NMOS mold source layer 13a and the drain layer 13 -- p+ of b and PMOS Mold source layer 18a and drain layer 18b are formed. Moreover, p+ of IGBT p+ of the mold contact layer 5 and NMOS Mold contact layer 13c is formed by the ion implantation.
[0054] Then, n+ of IGBT The mold source layer 4 and p+ The drain electrode 9 is formed in the source electrode 8 and p mold drain layer 1 at the mold contact layer 5. To source layer 13a of NMOS, drain layer 13b, and contact layer 13c, respectively Source electrode 17a, Drain electrode 17b and contact electrode 17c are formed, source electrode 22a and drain electrode 22b are formed in source layer 18a of PMOS, and drain layer 18b, respectively, and the high proof-pressure semiconductor device of this operation gestalt is completed.
[0055] (2nd operation gestalt) Drawing 2 is the sectional view showing the high proof-pressure semiconductor device concerning the 2nd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1 , and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that a part of epitaxial single-crystal-silicon layer is formed on an insulating-layer pattern, and the drain layer of NMOS and a part of channel field are formed in a part of this single-crystal-silicon layer.
[0056] As shown in drawing 2 , the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.
[0057] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, the polycrystal (Pori) silicon layer is prepared on the insulating-layer pattern 11. NMOS is formed in the epitaxial single-crystal-silicon layer 12, PMOS is formed in the polish recon layer on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12b.
[0058] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 31a and drain layer 31b of a mold, The channel field 32 formed among these, the gate electrode 34 formed through the gate insulating layer 33 on this, and p+ adjoined and formed in source layer 31a Contact layer 31c of a mold, It consists of drain electrode 35b in contact with source electrode 35a in contact with source layer 31a and contact layer 31c, and drain layer 31b. A part

of drain layer 31b of NMOS and channel field 32 are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and source layer 31a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0059] On the other hand, PMOS is n+ formed in the polish recon layer. It consists of source electrode 45a and drain electrode 45b which contact source layer 41a of a mold and drain layer 41b, the channel field 42 formed among these, the gate electrode 44 formed through the gate insulating layer 43 on this, source layer 41a, and drain layer 41b, respectively.

[0060] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0061] Also in this operation gestalt, like the 1st operation gestalt, it applies on the insulating-layer pattern 11 from p mold base layer 3 of a silicon substrate, and an amorphous silicon layer is formed, and this amorphous silicon layer is single-crystal-ized, using a silicon substrate as seed crystal. By this single crystal-ization, a part of part near seed crystal also single-crystal-izes the amorphous silicon layer on the insulating-layer pattern 11. By forming a part of channel field 32 of NMOS, and drain layer 31b in the part of this single-crystal-ized amorphous silicon layer, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 31b for the channel field 32 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case.

[0062] p mold drain layer 1 of IGBT prepared in the silicon substrate further again since the insulating-layer pattern 11 intervened between the silicon substrate and the epitaxial single-crystal-silicon layer 12, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 31b of a mold.

[0063] in addition, the 1st operation gestalt -- the same -- p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms -- having -- this p+ The channel field 32, source layer 31a, and contact layer 31c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 31a of a mold.

[0064] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0065] (3rd operation gestalt) Drawing 3 is the sectional view showing the high proof-pressure semiconductor device concerning the 3rd operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 2 , and detailed explanation is omitted. The point that this operation gestalt differs from the 2nd operation gestalt is a point that the drain layer of NMOS, all of channel fields, and a part of source layer are formed in a part of epitaxial single-crystal-silicon layer formed on the insulating-layer pattern.

[0066] As shown in drawing 3 , the trench gate mold vertical mold IGBT is formed in the semiconductor substrate as a high proof-pressure semiconductor device, and the CMOS mold semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.

[0067] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and on this insulating-layer pattern 11, as it runs aground in part, the epitaxial single-crystal-silicon layer 12 is formed on p mold base layer 3. Moreover, on the insulating-layer pattern 11, 12f of polycrystal (Pori) silicon layers is prepared. NMOS is formed in the epitaxial single-crystal-silicon

layer 12, PMOS (not shown) is formed in 12f of polish recon layers on the insulating-layer pattern 11, respectively, and NMOS and PMOS are divided into each other by isolation insulator layer 12c.

[0068] That is, NMOS is n+ formed in the epitaxial single-crystal-silicon layer 12. Source layer 51a and drain layer 51b of a mold, The channel field 52 formed among these, the gate electrode 54 formed through the gate insulating layer 53 on this, and p+ adjoined and formed in source layer 51a Contact layer 51c of a mold, It consists of drain electrode 55b in contact with source electrode 55a in contact with source layer 51a and contact layer 51c, and drain layer 51b. A part for drain layer 51b of NMOS and all of the channel fields 52 and a part of source layer 51a are formed in a part of epitaxial single-crystal-silicon layer 12 on the insulating-layer pattern 11, and a part of source layer 51a is formed in a part of epitaxial single-crystal-silicon layer 12 of p mold base layer 3 front face where the insulating-layer pattern 11 does not exist.

[0069] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS and good PMOS can be obtained like the 1st operation gestalt, and increase of leakage current can be prevented. Moreover, it is also possible to rationalize the threshold of NMOS.

[0070] Also in this operation gestalt, the amorphous silicon layer formed on the insulating-layer pattern 11 from p mold base layer 3 of a silicon substrate, having applied is single-crystal-ized like the 2nd operation gestalt, using a silicon substrate as seed crystal. When a part of part also with the amorphous silicon layer near seed crystal on the insulating-layer pattern 11 single-crystal-izes and forms a part for drain layer 51b of NMOS, and all of the channel fields 52, and a part of source layer 51a in the part of this single-crystal-ized amorphous silicon layer by this single crystal-ization, it is possible to prevent increase of the leakage current of NMOS certainly. Since especially the channel field 52 is close to the silicon substrate used as seed crystal, it is possible to acquire the crystallinity which may be set to the channel field 52, and the effectiveness of leakage current prevention is large. Furthermore, it is also possible to form in the polish recon field to which that point did not single-crystal-ize drain layer 51b for the channel field 52 of NMOS to the single crystal-ized field of an amorphous silicon layer, and increase of the leakage current of NMOS can be prevented also in this case. Moreover, since the channel field 52 of NMOS is completely insulated from the silicon substrate with this structure, as for this channel field 52, it is hard to be influenced of the potential of a silicon substrate, and a setup of a threshold and control become easy.

[0071] p mold drain layer 1 of IGBT prepared in the silicon substrate with the insulating-layer pattern 11 further again, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by drain layer 51b of a mold.

[0072] in addition, the 1st operation gestalt -- the same -- p+ of high concentration [front face / of p mold base layer 3 / layer / 3 / concerned / p mold base] a mold diffusion layer forms -- having -- this p+ Source layer 51a and contact layer 51c may be made to be formed in the front face of a mold diffusion layer. p mold drain layer 1 of IGBT which this prepared in the silicon substrate like the 1st operation gestalt, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 51a of a mold.

[0073] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.

[0074] (4th operation gestalt) Drawing 4 is the sectional view showing the high proof-pressure semiconductor device concerning the 4th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 1 , and detailed explanation is omitted. The point that this operation gestalt differs from the 1st operation gestalt is a point that NMOS is formed in p mold base layer of IGBT of a silicon substrate, and high-concentration p type layer is formed between this NMOS and p mold base layer.

[0075] As shown in drawing 4 , the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the CMOS mold

semiconductor device described below is formed on the same chip as this high proof-pressure semiconductor device.
[0076] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and 12g of polycrystal (Pori) silicon layers is prepared on this insulating-layer pattern 11. PMOS is formed in 12g of this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and PMOS are divided into each other by 12d of isolation insulator layers.
[0077] That is, NMOS is n+ formed in p type semiconductor layer 3b. Source layer 61a and drain layer 61b of a mold, The channel field 62 formed among these, the gate electrode 64 formed through the gate insulating layer 63 on this, and p+ adjoined and formed in source layer 61a Contact layer 61c of a mold, It consists of drain electrode 65b in contact with source electrode 65a in contact with source layer 61a and contact layer 61c, and drain layer 61b. p+ of high concentration [b / under Above NMOS / p type semiconductor layer 3/ layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.
[0078] On the other hand, PMOS is n+ formed in 12g of polish recon layers. It consists of source electrode 75a and drain electrode 75b which contact source layer 71a of a mold and drain layer 71b, the channel field 72 formed among these, the gate electrode 74 formed through the gate insulating layer 73 on this, source layer 71a, and drain layer 71b, respectively.
[0079] According to this operation gestalt, since NMOS is formed in p type semiconductor layer 3b of a silicon substrate, NMOS will be formed in the crystalline good single crystal part, good NMOS and good PMOS can be obtained in channel mobility and saturation characteristics like the 1st operation gestalt, and increase of leakage current can be prevented.
[0080] Moreover, since NMOS is formed in the low-concentration p type semiconductor layer 3 rather than p mold base layer 3 of IGBT, it is also possible to rationalize the threshold of the NMOS concerned. Formation of this p type semiconductor layer 3 is performed in advance of formation of p mold base layer of IGBT.
[0081] p+ of high concentration [layer / 3 / p type semiconductor layer 3b or / p mold base] further again p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 61a of a mold or drain layer 61b.
[0082] Thus, according to this operation gestalt, since good NMOS and a PMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.
[0083] (5th operation gestalt) Drawing 5 is the sectional view showing the high proof-pressure semiconductor device concerning the 5th operation gestalt of this invention. The same sign is attached and shown in the same part as drawing 4 , and detailed explanation is omitted. The point that this operation gestalt differs from the 4th operation gestalt is a point that diode is formed in the polycrystal (Pori) silicon layer formed on the insulating-layer pattern.
[0084] As shown in drawing 5 , the trench gate mold vertical mold IGBT is formed in the semi-conductor substrate as a high proof-pressure semiconductor device, and the diode described below is formed on the same chip as this high proof-pressure semiconductor device.
[0085] That is, on a silicon substrate, the insulating-layer pattern 11 is formed alternatively, and the polycrystal (Pori) silicon layer is prepared on this insulating-layer pattern 11. Diode is formed in this polish recon layer. Moreover, rather than p mold base layer 3, low-concentration p type semiconductor layer 3b is formed alternatively, and NMOS is formed in the field in which NMOS in p mold base layer 3 is formed at this p type semiconductor layer 3b. NMOS and diode are divided into each other by isolation insulator layer 12e.
[0086] That is, NMOS is n+ formed in p type semiconductor layer 3b. Source layer 81a and drain layer 81b of a mold, The channel field 82 formed among these, the gate electrode 84 formed through the gate insulating layer 83 on this, and p+ adjoined and formed in source layer 81a Contact layer 81c of a mold, It consists of drain electrode 85b in contact with source electrode 85a in contact with source layer 81a and contact layer 81c, and drain layer 81b. p+ of high

concentration [b / under Above NMOS / p type semiconductor layer 3/ layer / 3 / p type semiconductor layer 3b / concerned / or / p mold base] Mold diffusion layer 3c is formed.
[0087] On the other hand, diode is p+ formed in the polish recon layer. Anode layer 91a of a mold, and n+ It consists of anode electrode 92a and cathode electrode 92b which contact cathode layer 91b of a mold, anode layer 91a, and cathode layer 91b, respectively.
[0088] According to this operation gestalt, in channel mobility and saturation characteristics, good NMOS can be obtained like the 4th operation gestalt, and increase of leakage current can be prevented.
[0089] Moreover, it is also possible to rationalize the threshold of NMOS by the p type semiconductor layer 3 like the 4th operation gestalt. Furthermore, p+ p mold drain layer 1 of IGBT prepared in the silicon substrate by mold diffusion layer 3c, n mold base layer 2, p mold base layer 3, and n+ of NMOS It is possible to be able to prevent that a parasitism thyristor is constituted and to control thyristor actuation of a component by source layer 81a of a mold or drain layer 81b.
[0090] Thus, according to this operation gestalt, since a good NMOS property can be acquired, it is possible to constitute analogs, such as a drive circuit and a protection network, and digital various circuits from high degree of accuracy in one with IGBT.
[0091] In addition, this invention is not limited to the above-mentioned operation gestalt. For example, p+ Between the mold drain layer 1 and n mold base layer 2, high-concentration n mold buffer layer can be formed rather than the n mold base layer 2 concerned, and it is possible to raise conductivity.
[0092] Moreover, although the above-mentioned operation gestalt explained the high proof-pressure semiconductor device of a vertical mold, this invention is applicable also to the high proof-pressure semiconductor device of a horizontal type. In this case, a drain layer is formed in the semi-conductor substrate front face of the same side as a source layer.
[0093] At the above-mentioned operation gestalt, it is p+ further again. It is a drain layer, although IGBT which has the drain layer of a mold was mentioned as the example and explained n+ It is also possible to consider as a mold and to apply to various quantity proof-pressure semiconductor devices, such as an MOS mold quantity proof-pressure semiconductor device and other thyristors. In addition, it is possible to deform variously and to carry out in the range which does not deviate from the meaning of this invention.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view showing the high proof-pressure semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 2] The sectional view showing the high proof-pressure semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 3] The sectional view showing the high proof-pressure semiconductor device concerning the 3rd operation gestalt of this invention.
[Drawing 4] The sectional view showing the high proof-pressure semiconductor device concerning the 4th operation gestalt of this invention.
[Drawing 5] The sectional view showing the high proof-pressure semiconductor device concerning the 5th operation gestalt of this invention.
[Drawing 6] The sectional view showing the conventional high proof-pressure semiconductor device.
[Drawing 7] The property Fig. having shown the relation between the electrical potential difference of NMOS and PMOS, and a current.
[Description of Notations]
1 P+ Mold Drain Layer
2 N Mold Base Layer
3 P Mold Base Layer
3a Trench
4 N+ Mold Source Layer
5 P+ Mold Contact Layer
6 Gate Dielectric Film
7 Gate Electrode
8 Source Electrode
9 Drain Electrode
10 P+ Mold Diffusion Layer
11 Insulating-Layer Pattern
12 Epitaxial Single-Crystal-Silicon Layer
12a Isolation insulator layer
13a n+ Source layer of a mold
13b n+ Drain layer of a mold
13c Contact layer
14 Channel Field
15 Gate Insulating Layer
16 Gate Electrode
17a Source electrode
17b Drain electrode
17c Contact electrode
18a n+ Source layer of a mold
18b Drain layer

19 Channel Field
20 Gate Insulating Layer
21 Gate Electrode
22a Source electrode
22b Drain electrode

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（Ａ）　(11)特許出願公開番号
特開2000－150664
（P2000－150664A）
(43)公開日　平成12年５月30日(2000.5.30)

(51)Int.Cl.⁷	識別記号	ＦＩ		テーマコード（参考）
Ｈ０１Ｌ 21/8234		Ｈ０１Ｌ 27/08	１０２Ａ	５Ｆ０３８
27/088		27/04	Ｈ	５Ｆ０４０
27/04		27/08	３２１Ａ	５Ｆ０４８
21/822		29/78	３０１Ｊ	５Ｆ１１０
21/8238			３０１Ｋ	

審査請求　未請求　請求項の数19　ＯＬ　（全 13 頁）　最終頁に続く

(21)出願番号　特願平10－324609

(22)出願日　平成10年11月16日(1998.11.16)

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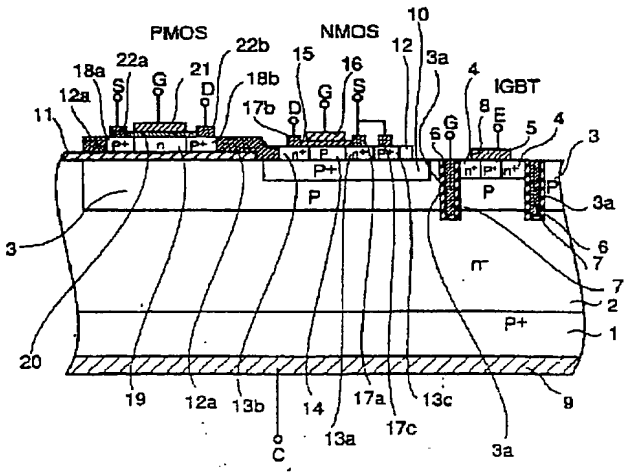
(54)【発明の名称】　高耐圧半導体装置

(57)【要約】
【課題】　高耐圧素子及びドライブ回路や保護回路等を一体化した高耐圧半導体装置を信頼性高く低コストで提供すること。
【解決手段】　半導体基板表面に積層されたエピタキシャル単結晶半導体層１０に形成されたソース層１３ａ、ドレイン層１３ｂと、ゲート絶縁膜１５と、ゲート電極１６とを有するｎ型のＭＯＳ型半導体素子と、前記半導体基板上に絶縁膜１１を介して積層された多結晶半導体層に形成されたソース層１８ａ、ドレイン層１８ｂと、ゲート絶縁膜２０と、ゲート電極２１とを有するｐ型の第２のＭＯＳ型半導体素子と、前記半導体基板に形成されたＩＧＢＴ等の高耐圧半導体素子とを具備する。



【特許請求の範囲】

【請求項１】　半導体基板表面に形成された第１のソース層及び第１のドレイン層と、当該第１のソース層と第１のドレイン層間の前記半導体基板表面に第１のゲート絶縁膜を介して形成された第１のゲート電極とを有するｎ型の第１のＭＯＳ型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第２のソース層及び第２のドレイン層と、当該第２のソース層と第２のドレイン層間の前記多結晶半導体層表面に第２のゲート絶縁膜を介して形成された第２のゲート電極とを有するｐ型の第２のＭＯＳ型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置。

【請求項２】　前記高耐圧半導体素子は、前記半導体基板に形成されたｎ型のベース層と、このｎ型のベース層の表面に形成されたｐ型のベース層と、このｐ型のベース層の表面に形成されたｎ型の第３のソース層及びｐ型のコンタクト層と、前記ｐ型のベース層の表面に第３のゲート絶縁膜を介して形成された第３のゲート電極と、前記ｎ型のベース層の表面のうち前記ｐ型のベース層から離れた位置に形成された第３のドレイン層と、前記第３のソース層及び前記ｐ型のコンタクト層に接する第１のコンタクト電極と、前記第３のドレイン層に接する第２のコンタクト電極とを備えることを特徴とする請求項１記載の高耐圧半導体装置。

【請求項３】　前記第１のソース層及び第１のドレイン層は、前記ｐ型のベース層の表面に形成されていることを特徴とする請求項２記載の高耐圧半導体装置。

【請求項４】　前記第１のソース層及び第１のドレイン層と前記ｐ型のベース層との間には、当該ｐ型のベース層よりも高濃度のｐ型の半導体層が形成されていることを特徴とする請求項３記載の高耐圧半導体装置。

【請求項５】　半導体基板表面に積層されたエピタキシャル単結晶半導体層に形成された第１のソース層及び第１のドレイン層と、当該第１のソース層と第１のドレイン層間の前記半導体基板表面に第１のゲート絶縁膜を介して形成された第１のゲート電極とを有するｎ型の第１のＭＯＳ型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第２のソース層及び第２のドレイン層と、当該第２のソース層と第２のドレイン層間の前記多結晶半導体層表面に第２のゲート絶縁膜を介して形成された第２のゲート電極とを有するｐ型の第２のＭＯＳ型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置。

【請求項６】　前記高耐圧半導体素子は、前記半導体基板に形成されたｎ型のベース層と、このｎ型のベース層の表面に形成されたｐ型のベース層と、このｐ型のベース層の表面に形成されたｎ型の第３のソース層及びｐ型のコンタクト層と、前記ｐ型のベース層の表面に第３のゲート絶縁膜を介して形成された第３のゲート電極と、前記ｎ型のベース層の表面のうち前記ｐ型のベース層から離れた位置に形成された第３のドレイン層と、前記第３のソース層及び前記ｐ型のコンタクト層に接する第１のコンタクト電極と、前記第３のドレイン層に接する第２のコンタクト電極とを備えることを特徴とする請求項５記載の高耐圧半導体装置。

【請求項７】　前記エピタキシャル単結晶半導体層は、前記ｐ型のベース層の表面に形成されていることを特徴とする請求項６記載の高耐圧半導体装置。

【請求項８】　前記第１のソース層及び第１のドレイン層と前記ｐ型のベース層との間には、当該ｐ型のベース層よりも高濃度のｐ型の半導体層が形成されていることを特徴とする請求項７記載の高耐圧半導体装置。

【請求項９】　半導体基板上に絶縁膜が形成され、前記半導体基板表面から前記絶縁膜上にわたってエピタキシャル成長した半導体層に形成された第１のソース層及び第１のドレイン層と、当該第１のソース層と第１のドレイン層間の前記半導体層表面に第１のゲート絶縁膜を介して形成された第１のゲート電極とを有するｎ型の第１のＭＯＳ型半導体素子と、前記半導体層の前記絶縁膜上の部分に形成された第２のソース層及び第２のドレイン層と、この第２のソース層と第２のドレイン層間の前記半導体層表面に第２のゲート絶縁膜を介して形成された第２のゲート電極とを有するｐ型の第２のＭＯＳ型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置。

【請求項１０】　前記第１のＭＯＳ型半導体素子の第１のソース層は前記エピタキシャル成長した半導体層の前記半導体基板表面の部分に、当該素子の第１のドレイン層は前記半導体層の前記絶縁膜上の部分に、それぞれ形成されていることを特徴とする請求項９記載の高耐圧半導体装置。

【請求項１１】　前記高耐圧半導体素子は、前記半導体基板に形成されたｎ型のベース層と、このｎ型のベース層の表面に形成されたｐ型のベース層と、このｐ型のベース層の表面に形成されたｎ型の第３のソース層及びｐ型のコンタクト層と、前記ｐ型のベース層の表面に第３のゲート絶縁膜を介して形成された第３のゲート電極と、前記ｎ型のベース層の表面のうち前記ｐ型のベース層から離れた位置に形成された第３のドレイン層と、前記第３のソース層及び前記ｐ型のコンタクト層に接する第１のコンタクト電極と、前記第３のドレイン層に接する第２のコンタクト電極とを備えることを特徴とする請求項９又は１０記載の高耐圧半導体装置。

【請求項１２】　前記エピタキシャル成長した半導体層の前記第１のソース層が形成された部分は、前記ｐ型のベース層の表面に形成されていることを特徴とする請求項１１記載の高耐圧半導体装置。

【請求項１３】　前記第１のソース層と前記ｐ型のベー

ス層との間には、当該ｐ型のベース層よりも高濃度のｐ型の半導体層が形成されていることを特徴とする請求項１２記載の高耐圧半導体装置。

【請求項１４】　前記エピタキシャル成長した半導体層は単結晶からなり、前記半導体層の前記絶縁膜上の部分は多結晶からなることを特徴とする請求項９乃至１３記載の高耐圧半導体装置。

【請求項１５】　前記第３のドレイン層はｐ型層であることを特徴とする請求項２乃至４、６乃至８、又は１１乃至１４記載の高耐圧半導体装置。

【請求項１６】　前記高耐圧半導体素子は縦型の半導体素子であり、前記第３のドレイン層は前記第３のソース層に対して反対側の前記ｎ型のベース層の表面に形成されていることを特徴とする請求項２乃至４、６乃至８、１１乃至１５記載の高耐圧半導体装置。

【請求項１７】　前記第３のソース層及び前記ｐ型のベース層を貫き前記ｎ型のベース層に達するように溝が形成され、この溝の中に前記第３のゲート絶縁膜を介して前記第３のゲート電極が埋め込まれていることを特徴とする請求項２乃至４、６乃至８、１１乃至１６記載の高耐圧半導体装置。

【請求項１８】　前記ｎ型のベース層と前記第３のドレイン層との間には、当該ｎ型のベース層よりも高濃度のｎ型の半導体層が形成されていることを特徴とする請求項２乃至４、６乃至８、１１乃至１７記載の高耐圧半導体装置。

【請求項１９】　前記ｎ型の第１のＭＯＳ型半導体素子と前記ｐ型の第２のＭＯＳ型半導体素子とはＣＭＯＳ回路を構成することを特徴とする請求項１乃至１８記載の高耐圧半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、高耐圧半導体装置に係わり、特にＭＯＳ型半導体素子を有する高耐圧縦型半導体装置に関する。

【０００２】

【従来の技術】ＩＧＢＴ（Insulated Gate Bipolar Transistor）等の高耐圧素子はモータ制御、電源など多くの産業分野で使用されている。かかる高耐圧素子は大電力を扱うために、シリコン基板の表面と裏面をカソード、アノードまたはエミッタ、コレクタとする縦型素子が多く使われている。

【０００３】このようなＩＧＢＴ等の高耐圧素子、特に縦型素子を使い易くするためにドライブ回路や保護回路を一体化させ、高耐圧素子を壊れにくく、かつ高性能化することが行われている。通常このような回路はＩＧＢＴ等の高耐圧素子のチップとは別に作られ、同一パッケージに搭載するというモジュールの形態が採られる。

【０００４】同一チップ上にこれらの回路を搭載できればコストと信頼性の面で飛躍的に有利になるが、従来技術ではこれを容易に達成する手段がなかった。例えば、同一チップ上にドライブ回路や保護回路、例えばＣＭＯＳ回路等を作った場合には、ＩＧＢＴ内部にキャリアプラズマが存在するため、ｎ型ＭＯＳトランジスタ（以下、ＮＭＯＳと略称する。）、ｐ型ＭＯＳトランジスタ（以下、ＰＭＯＳと略称する。）が簡単にラッチアップしてしまうという問題がある。

【０００５】また、上記問題を解決するため、半導体基板に設けたＩＧＢＴ上に絶縁膜を介してポリシリコン層を形成し、このポリシリコン層にＣＭＯＳ回路を設けた高耐圧半導体装置がある。図６は、この高耐圧半導体装置の構造を示す断面図である。

【０００６】図６に示すように、この高耐圧半導体装置はトレンチゲート型縦型高耐圧半導体装置である。半導体基板には高抵抗のｎ型ベース層２が形成されており、このｎ型ベース層２の一面には高濃度のｐ型ドレイン層１が形成されている。ｐ型ドレイン層１にはドレイン電極９がコンタクトしている。また、ｎ型ベース層２の他方の面にはｐ型ベース層３が形成されており、このｐ型ベース層３の表面には高濃度のｎ型ソース層４及び高濃度のｐ型コンタクト層５が形成されている。

【０００７】さらに、上記半導体基板表面には複数のトレンチ３ａが形成されている。これらのトレンチ３ａはストライプ状の上面形状で互いに平行に配列されており（図示せず。）、ｎ型ソース層４及びｐ型ベース層３を貫通してｎ型ベース層２に到達するように形成されている。複数のトレンチ３ａの中にはゲート絶縁膜６を介してゲート電極７が埋め込まれている。

【０００８】図６でも明らかなように、複数のトレンチ３ａ間の半導体基板表面の領域には上記ｎ型ソース層４がゲート絶縁膜６と接して形成されており、ｎ型ソース層４に囲まれるようにしてｐ型コンタクト層５が形成されている。また、ｎ型ソース層４及びｐ型コンタクト層５に接してソース電極８がコンタクトしている。

【０００９】以上のように、高耐圧半導体素子としてトレンチゲート型縦型ＩＧＢＴが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるＣＭＯＳ型半導体素子が形成されている。

【００１０】即ち、ｐ型ベース層３上には絶縁膜１２１を介して多結晶（ポリ）シリコン層１２２が形成され、このポリシリコン層１２２にはＮＭＯＳ及びＰＭＯＳが形成されており、さらにＮＭＯＳとＰＭＯＳとは素子分離絶縁膜１２２ａによりお互いに分離されている。

【００１１】ＮＭＯＳは、ポリシリコン層１２２に形成されたソース層１０１ａ及びドレイン層１０１ｂ、これらの間に形成されたチャネル領域１０２、この上にゲート絶縁層１０３を介して形成されたゲート電極１０４、ソース層１０１ａ及びドレイン層１０１ｂにそれぞれコンタクトするソース電極１０５ａ及びドレイン電極１０５ｂから構成されている。

【００１２】一方、ＰＭＯＳは、ポリシリコン層１２２に形成されたソース層１１１ａ及びドレイン層１１１ｂ、これらの間に形成されたチャネル領域１１２、この上にゲート絶縁層１１３を介して形成されたゲート電極１１４、ソース層１１１ａ及びドレイン層１１１ｂにそれぞれコンタクトするソース電極１１５ａ及びドレイン電極１１５ｂから構成されている。

【００１３】以上のようにして同一チップ上にＩＧＢＴ及びＣＭＯＳ回路を一応搭載することはできる。しかしながら、半導体基板上に設けたポリシリコン層に形成したＣＭＯＳ半導体素子は特性が悪く、高精度のアナログ回路を組むことができないという問題が生ずる。

【００１４】即ち、ポリシリコン層に形成したＰＭＯＳは比較的良好な特性が得られるが、同じくポリシリコン層に形成したＮＭＯＳは単結晶シリコン層に形成したＮＭＯＳと比べてチャネル移動度が低く、飽和特性も得られない。図７は、ポリシリコン層に形成したＮＭＯＳ及びＰＭＯＳのソース・ドレイン間電圧（横軸）とドレイン電流（縦軸）との関係を示す特性図である。図７（ａ）はＮＭＯＳの場合の特性を示すもので、ソース・ドレイン間電圧の増加によりドレイン電流も増加し、飽和特性が得られないことがわかる。一方、図７（ｂ）はＰＭＯＳの場合の特性を示すもので、ソース・ドレイン間電圧の増加によりドレイン電流も増加するが、飽和特性が得られることがわかる。

【００１５】

【発明が解決しようとする課題】以上述べたように、高耐圧素子を使い易くするためにドライブ回路や保護回路を一体化させて、壊れにくく、かつ高性能化した高耐圧素子を信頼性高く低コストで提供することが試みられているが、従来技術ではこれを容易に達成する手段がなかった。

【００１６】例えば、同一チップ上にドライブ回路や保護回路、例えばＣＭＯＳ回路等を作った場合には、ＩＧＢＴ内部にキャリアプラズマが存在するため、ＮＭＯＳ及びＰＭＯＳが簡単にラッチアップしてしまうという問題がある。

【００１７】また、半導体基板上に設けたポリシリコン層に形成したＣＭＯＳ半導体素子は特性が悪く、高精度のアナログ回路を組むことができないという問題が生ずる。本発明は上記実情に鑑みてなされたものであり、高耐圧素子及びドライブ回路や保護回路等を一体化した高耐圧半導体装置を信頼性高く低コストで提供することを目的とするものである。

【００１８】

【課題を解決するための手段】前述した課題を解決するために、本発明の第１は、半導体基板表面に形成された第１のソース層及び第１のドレイン層と、当該第１のソース層と第１のドレイン層間の前記半導体基板表面に第１のゲート絶縁膜を介して形成された第１のゲート電極とを有するｎ型の第１のＭＯＳ型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第２のソース層及び第２のドレイン層と、当該第２のソース層と第２のドレイン層間の前記多結晶半導体層表面に第２のゲート絶縁膜を介して形成された第２のゲート電極とを有するｐ型の第２のＭＯＳ型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置を提供する。

【００１９】また本発明の第２は、半導体基板表面に積層されたエピタキシャル単結晶半導体層に形成された第１のソース層及び第１のドレイン層と、当該第１のソース層と第１のドレイン層間の前記半導体基板表面に第１のゲート絶縁膜を介して形成された第１のゲート電極とを有するｎ型の第１のＭＯＳ型半導体素子と、前記半導体基板上に絶縁膜を介して積層された多結晶半導体層に形成された第２のソース層及び第２のドレイン層と、当該第２のソース層と第２のドレイン層間の前記多結晶半導体層表面に第２のゲート絶縁膜を介して形成された第２のゲート電極とを有するｐ型の第２のＭＯＳ型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置を提供する。

【００２０】また本発明の第３は、半導体基板上に絶縁膜が形成され、前記半導体基板表面から前記絶縁膜上にわたってエピタキシャル成長した半導体層に形成された第１のソース層及び第１のドレイン層と、当該第１のソース層と第１のドレイン層間の前記半導体層表面に第１のゲート絶縁膜を介して形成された第１のゲート電極とを有するｎ型の第１のＭＯＳ型半導体素子と、前記半導体層の前記絶縁膜上の部分に形成された第２のソース層及び第２のドレイン層と、この第２のソース層と第２のドレイン層間の前記半導体層表面に第２のゲート絶縁膜を介して形成された第２のゲート電極とを有するｐ型の第２のＭＯＳ型半導体素子と、前記半導体基板に形成された高耐圧半導体素子とを具備することを特徴とする高耐圧半導体装置を提供する。

【００２１】上記した本発明において、以下の構成を具備することが好ましい。

（１）本発明の第１、２、３において、前記高耐圧半導体素子は、前記半導体基板に形成されたｎ型のベース層と、このｎ型のベース層の表面に形成されたｐ型のベース層と、このｐ型のベース層の表面に形成されたｎ型の第３のソース層及びｐ型のコンタクト層と、前記ｐ型のベース層の表面に第３のゲート絶縁膜を介して形成された第３のゲート電極と、前記ｎ型のベース層の表面のうち前記ｐ型のベース層から離れた位置に形成された第３のドレイン層と、前記第３のソース層及び前記ｐ型のコンタクト層に接する第１のコンタクト電極と、前記第３のドレイン層に接する第２のコンタクト電極とを備える

こと。

【００２２】（２）本発明の第１、２、３において、前記第３のドレイン層はｐ型層であること。

（３）本発明の第１、２、３において、前記高耐圧半導体素子は縦型の半導体素子であり、前記第３のドレイン層は前記第３のソース層に対して反対側の前記ｎ型のベース層の表面に形成されていること。

【００２３】（４）本発明の第１、２、３において、前記第３のソース層及び前記ｐ型のベース層を貫き前記ｎ型のベース層に達するように溝が形成され、この溝の中に前記第３のゲート絶縁膜を介して前記第３のゲート電極が埋め込まれていること。

【００２４】（５）本発明の第１、２、３において、前記ｎ型のベース層と前記第３のドレイン層との間には、当該ｎ型のベース層よりも高濃度のｎ型の半導体層が形成されていること。

【００２５】（６）本発明の第１、２、３において、前記ｎ型の第１のＭＯＳ型半導体素子と前記ｐ型の第２のＭＯＳ型半導体素子とはＣＭＯＳ回路を構成すること

（７）本発明の第１において、前記第１のソース層及び第１のドレイン層は、前記ｐ型のベース層の表面に形成されていること。

【００２６】（８）本発明の第２において、前記エピタキシャル単結晶半導体層は、前記ｐ型のベース層の表面に形成されていること。

（９）本発明の第１、２において、前記第１のソース層及び第１のドレイン層と前記ｐ型のベース層との間には、当該ｐ型のベース層よりも高濃度のｐ型の半導体層が形成されていること。

【００２７】（１０）本発明の第３において、前記第１のＭＯＳ型半導体素子の第１のソース層は前記エピタキシャル成長した半導体層の前記半導体基板表面の部分に、当該素子の第１のドレイン層は前記半導体層の前記絶縁膜上の部分に、それぞれ形成されていること。

【００２８】（１１）本発明の第３において、前記エピタキシャル成長した半導体層の前記第１のソース層が形成された部分は、前記ｐ型のベース層の表面に形成されていること。

【００２９】（１２）本発明の第３において、前記第１のソース層と前記ｐ型のベース層との間には、当該ｐ型のベース層よりも高濃度のｐ型の半導体層が形成されていること。

【００３０】（１３）本発明の第３において、前記エピタキシャル成長した半導体層は単結晶からなり、前記半導体層の前記絶縁膜上の部分は多結晶からなること。本発明においては、例えば、ＩＧＢＴ等の高耐圧半導体素子と同じシリコン基板上又はこの上に設けたエピタキシャル結晶層にＮＭＯＳを形成し、ＰＭＯＳは酸化膜上に設けたポリシリコン層上に設ける。

【００３１】ポリシリコン層に形成したＰＭＯＳは比較的良好な特性が得られるが、ＮＭＯＳをポリシリコン層に形成した場合は単結晶シリコンに形成したものと比べてチャネル移動度が低く、飽和特性も得られない。本発明によれば、ＩＧＢＴ等はｐベース拡散層を持つため、特に本発明の第１のように、このｐベース拡散層中に比較的容易にＮＭＯＳを形成することができる。この構成によれば良好なＮＭＯＳ特性を得ることが可能である。

【００３２】かかる構成では、ＩＧＢＴ等の内部に存在するプラズマのためリーク電流が大きくなってしまう場合があるので、以下に示す構成がより好ましい。即ち、ＮＭＯＳのｐベース電位がＩＧＢＴ等の高耐圧半導体素子のソース電位と同じになるように、当該ｐベースとソースとの間にショート電極を設けておくことが望ましい。

【００３３】また、本発明の第２及び第３においては、例えば、シリコン基板上にシリコン酸化膜パターンを設け、ｐベース上からこのシリコン酸化膜パターン上にかけてアモルファスシリコン層を設け、これを６００℃程度でアニールして結晶化する方法を用いることが可能である。この方法により、上記ｐベース上にはエピタキシャル成長シリコン層が形成され、この層にＮＭＯＳを作製することができ、また上記シリコン酸化膜パターン上にはポリシリコン層が形成され、この層にＰＭＯＳを作製することができる。その結果、かかるポリシリコン層に形成したＰＭＯＳ、及びエピタキシャル成長シリコン層に形成したＮＭＯＳともども、チャネル移動度及び飽和特性において良好な特性を得ることが可能となる。

【００３４】さらにまた、上記したシリコン酸化膜パターン上に延在させたアモルファスシリコン層の一部は、上記ｐベースに近い部分において、単結晶のエピタキシャル成長層とすることも可能である。したがって、この部分にＮＭＯＳのドレイン、チャネル（ベース）、又はソースを形成することが可能である。例えば、ＮＭＯＳのソースはｐベース上のエピタキシャル成長層に、チャネル（ベース）はシリコン酸化膜パターン上の単結晶エピタキシャル成長層に、ドレインは当該酸化膜パターン上のエピタキシャル成長層（単結晶若しくはポリシリコン）に設ける。

【００３５】かかる構成によれば、チャネル移動度及び飽和特性において良好な特性を得ることができ、リーク電流の増大を防止することができる。さらに、ドレインはシリコン酸化膜パターン上に存在するので、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層、高抵抗ｎ型層、ｐ型ベース層、及びＮＭＯＳのｎ型ソース層によって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００３６】以上のように、本発明のよれば、ＮＭＯＳを半導体基板、若しくはその上のエピタキシャル成長層に設け、ＰＭＯＳを絶縁膜上の多結晶層に設けるので、良好なＮＭＯＳ及びＰＭＯＳ特性を得ることができ、ド

ライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でＩＧＢＴ等の高耐圧半導体素子と一体的に構成することが可能である。

【００３７】

【発明の実施の形態】以下、本発明の高耐圧半導体装置に係る実施形態について図面を用いつつ詳細に説明する。

（第１の実施形態）図１は、本発明の第１の実施形態に係わる高耐圧半導体装置を示す断面図である。本実施形態の高耐圧半導体装置はトレンチゲート型縦型ＩＧＢＴである。

【００３８】図１に示すように、半導体基板（シリコン基板）には高抵抗のｎ型ベース層２が形成されており、このｎ型ベース層２の一面には高濃度のｐ$^+$型ドレイン層１が形成されている。ｐ型ドレイン層１にはドレイン電極９がコンタクトしている。また、ｎ型ベース層２の他方の面にはｐ型ベース層３が形成されており、このｐ型ベース層３の表面には高濃度のｎ$^+$型ソース層４及び高濃度のｐ$^+$型コンタクト層５が形成されている。

【００３９】さらに、上記半導体基板表面には複数のトレンチ３ａが形成されている。これらのトレンチ３ａはストライプ状の上面形状で互いに平行に配列されており（図示せず。）、ｎ$^+$型ソース層４及びｐ型ベース層３を貫通してｎ型ベース層２に到達するように形成されている。複数のトレンチ３ａの中にはゲート絶縁膜６を介してゲート電極７が埋め込まれている。

【００４０】図１でも明らかなように、複数のトレンチ３ａ間の半導体基板表面の領域には上記ｎ$^+$型ソース層４がゲート絶縁膜６と接して形成されており、ｎ$^+$型ソース層４に囲まれるようにしてｐ$^+$型コンタクト層５が形成されている。また、ｎ$^+$型ソース層４及びｐ$^+$型コンタクト層５に接してソース電極８がコンタクトしている。ｐ$^+$型コンタクト層５はトレンチ３ａ間に複数配置されていても良く、ｎ$^+$型ソース層４及びｐ$^+$型コンタクト層５に対するソース電極８のコンタクトを確実に取るため、当該ｎ$^+$型ソース層４及びｐ$^+$型コンタクト層５はトレンチ１ａの長手方向に沿って交互に配置されていることが望ましい。

【００４１】以上のように、高耐圧半導体素子としてトレンチゲート型縦型ＩＧＢＴが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるＣＭＯＳ型半導体素子が形成されている。

【００４２】即ち、ｐ型ベース層３の表面には当該ｐ型ベース層３よりも高濃度のｐ$^+$型拡散層１０が形成され、このｐ$^+$型拡散層１０上にエピタキシャル単結晶シリコン層１２が設けられている。一方、ｐ$^+$型拡散層１０と異なる領域には絶縁層パターン１１が形成され、この絶縁層パターン１１上には多結晶（ポリ）シリコン層が設けられている。エピタキシャル単結晶シリコン層１２にはＮＭＯＳが、絶縁層パターン１１上のポリシリコン層にはＰＭＯＳがそれぞれ形成されており、ＮＭＯＳとＰＭＯＳとは素子分離絶縁膜１２ａによりお互いに分離されている。

【００４３】即ち、ＮＭＯＳは、エピタキシャル単結晶シリコン層１２に形成されたｎ$^+$型のソース層１３ａ及びドレイン層１３ｂ、これらの間に形成されたチャネル領域１４、この上にゲート絶縁層１５を介して形成されたゲート電極１６、ソース層１３ａに隣接して形成されたｐ$^+$型のコンタクト層１３ｃ、ソース層１３ａ、ドレイン層１３ｂ、及びコンタクト層１３ｃにそれぞれコンタクトするソース電極１７ａ、ドレイン電極１７ｂ、及びコンタクト電極１７ｃから構成されている。ソース電極１７ａとコンタクト電極１７ｃとはお互いに電気的に接続されている。

【００４４】一方、ＰＭＯＳは、ポリシリコン層に形成されたｎ+ 型のソース層１８ａ及びドレイン層１８ｂ、これらの間に形成されたチャネル領域１９、この上にゲート絶縁層２０を介して形成されたゲート電極２１、ソース層１８ａ及びドレイン層１８ｂにそれぞれコンタクトするソース電極２２ａ及びドレイン電極２２ｂから構成されている。

【００４５】以上のように、本実施形態においては、ＩＧＢＴが形成されたシリコン基板上にエピタキシャル単結晶シリコン層１２を設け、この結晶層１２にＮＭＯＳを形成するとともに、ＰＭＯＳは酸化膜１１上に形成されたポリシリコン層上に設ける。ポリシリコン層に形成したＰＭＯＳは比較的良好な特性が得られるが、ＮＭＯＳをポリシリコン層に形成した場合は単結晶シリコンに形成したものと比べてチャネル移動度が低く、飽和特性も得られない。しかしながら、本実施形態によれば、チャネル移動度及び飽和特性において良好なＮＭＯＳ及びＰＭＯＳを得ることができ、リーク電流の増大を防止することができる。

【００４６】また、ＮＭＯＳはｐ型ベース層３上の結晶化したアモルファスシリコン層１０に形成されるので、閾値は適正になる。即ち、通常のＩＧＢＴのｐ型ベース層の表面濃度はＮＭＯＳには高すぎる場合があるが、ドープされていないアモルファスシリコン層をｐ型ベース層上に形成すると、ｐ型不純物がｐ型ベース層から結晶化アモルファスシリコン層１０に拡散しても、当該ｐ型ベース層の表面濃度はＩＧＢＴのｐ型ベース層のそれよりも低くなり、ＮＭＯＳの閾値が適正化される。

【００４７】さらにまた、ｐ$^+$型拡散層１０がシリコン基板とエピタキシャル単結晶シリコン層１２との間に介在するので、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層１、ｎ型ベース層２、ｐ型ベース層３、及びＮＭＯＳのｎ$^+$型のソース層１３ａ又はドレイン層１３ｂによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００４８】このように、本実施形態によれば、良好な

ＮＭＯＳ及びＰＭＯＳ特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でＩＧＢＴと一体的に構成することが可能である。

【００４９】以上述べた本実施形態による高耐圧半導体装置の製造方法は、以下に述べる通りである。まず、縦型ＩＧＢＴのトレンチ１ａを形成するに先立ち、半導体基板のｐ型ベース層３の表面にｐ$^+$型拡散層１０を形成し、このｐ$^+$型拡散層１０及びＩＧＢＴ形成予定領域を除く領域に選択的に酸化膜１１を、例えばＬＯＣＯＳ法によって形成する。ここで、酸化膜１１を形成した後、この酸化膜１１等をマスクにしてイオン注入等によりｐ$^+$型拡散層１０を形成しても良い。

【００５０】次に、ｐ型ベース層３表面のｐ$^+$型拡散層１０から酸化膜１１上にかけてアモルファスシリコン（ａ－Ｓｉ）層を０．５μｍ程度堆積させ、６００℃で２０時間程度アニールして固相成長させる。このアニールによりｐ$^+$型拡散層１０上のアモルファスシリコン層は単結晶化してエピタキシャル単結晶シリコン層１２となる一方、酸化膜１１上のアモルファスシリコン層はポリシリコン層となる。

【００５１】この後、イオン注入により、エピタキシャル単結晶シリコン層１２のＮＭＯＳが形成される領域にはｐ型不純物を、前記ポリシリコン層のＰＭＯＳが形成される領域にはｎ型不純物をそれぞれ導入して、それぞれｐ型半導体層１４及びｎ型半導体層１９とする。さらに、エピタキシャル単結晶シリコン層１２のＮＭＯＳが形成される領域及び前記ポリシリコン層のＰＭＯＳが形成される領域を除く領域を酸化することにより、酸化部分にこれらの素子を分離する素子分離酸化膜１２ａを形成する。

【００５２】次に、ＩＧＢＴのゲートを形成するためにトレンチ３ａをシリコン基板に形成する。トレンチ３ａの内面にはゲート酸化膜６を、エピタキシャル単結晶シリコン層１２及び上記ポリシリコン層の表面にはＮＭＯＳ及びＰＭＯＳのゲート酸化膜（１５、２０）をそれぞれ同時に形成する。さらに、この上にトレンチを埋め込むようにポリシリコン膜を堆積し、ＩＧＢＴのゲート電極７を作製する。このポリシリコン膜は同時にＮＭＯＳ及びＰＭＯＳのゲート酸化膜（１５、２０）上にも堆積して、ＮＭＯＳ及びＰＭＯＳのゲート電極（１６、２１）をも形成することができる。

【００５３】次に、ゲート電極７、ゲート電極（１６、２１）をマスクとして、それぞれイオン注入によりＩＧＢＴのｎ$^+$型ソース層４、ＮＭＯＳのｎ$^+$型ソース層１３ａ及びドレイン層１３ｂ、ＰＭＯＳのｐ$^+$型ソース層１８ａ及びドレイン層１８ｂを形成する。また、ＩＧＢＴのｐ$^+$型コンタクト層５及びＮＭＯＳのｐ$^+$型コンタクト層１３ｃをイオン注入により形成する。

【００５４】この後、ＩＧＢＴのｎ$^+$型ソース層４及びｐ$^+$型コンタクト層５にはソース電極８、ｐ型ドレイン層１にはドレイン電極９を形成し、ＮＭＯＳのソース層１３ａ、ドレイン層１３ｂ、及びコンタクト層１３ｃにはそれぞれソース電極１７ａ、ドレイン電極１７ｂ、及びコンタクト電極１７ｃを形成し、ＰＭＯＳのソース層１８ａ及びドレイン層１８ｂにはそれぞれソース電極２２ａ及びドレイン電極２２ｂを形成して、本実施形態の高耐圧半導体装置が完成する。

【００５５】（第２の実施形態）図２は、本発明の第２の実施形態に係わる高耐圧半導体装置を示す断面図である。図１と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第１の実施形態と異なる点は、エピタキシャル単結晶シリコン層の一部分が絶縁層パターン上に形成され、この単結晶シリコン層の一部分にＮＭＯＳのドレイン層及びチャネル領域の一部が形成されている点である。

【００５６】図２に示すように、高耐圧半導体素子としてトレンチゲート型縦型ＩＧＢＴが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるＣＭＯＳ型半導体素子が形成されている。

【００５７】即ち、シリコン基板上には選択的に絶縁層パターン１１が形成され、この絶縁層パターン１１上に一部乗り上げるようにしてｐ型ベース層３上にエピタキシャル単結晶シリコン層１２が設けられている。また、絶縁層パターン１１上には多結晶（ポリ）シリコン層が設けられている。エピタキシャル単結晶シリコン層１２にはＮＭＯＳが、絶縁層パターン１１上のポリシリコン層にはＰＭＯＳがそれぞれ形成されており、ＮＭＯＳとＰＭＯＳとは素子分離絶縁膜１２ｂによりお互いに分離されている。

【００５８】即ち、ＮＭＯＳは、エピタキシャル単結晶シリコン層１２に形成されたｎ$^+$型のソース層３１ａ及びドレイン層３１ｂ、これらの間に形成されたチャネル領域３２、この上にゲート絶縁層３３を介して形成されたゲート電極３４、ソース層３１ａに隣接して形成されたｐ$^+$型のコンタクト層３１ｃ、ソース層３１ａ及びコンタクト層３１ｃにコンタクトするソース電極３５ａ、ドレイン層３１ｂにコンタクトするドレイン電極３５ｂから構成されている。ＮＭＯＳのドレイン層３１ｂ及びチャネル領域３２の一部は絶縁層パターン１１上のエピタキシャル単結晶シリコン層１２の一部分に形成され、ソース層３１ａは絶縁層パターン１１が存在しないｐ型ベース層３表面のエピタキシャル単結晶シリコン層１２の一部分に形成されている。

【００５９】一方、ＰＭＯＳは、ポリシリコン層に形成されたｎ$^+$型のソース層４１ａ及びドレイン層４１ｂ、これらの間に形成されたチャネル領域４２、この上にゲート絶縁層４３を介して形成されたゲート電極４４、ソース層４１ａ及びドレイン層４１ｂにそれぞれコンタクトするソース電極４５ａ及びドレイン電極４５ｂから構

成されている。

【００６０】本実施形態によれば、第１の実施形態と同様にチャネル移動度及び飽和特性において良好なＮＭＯＳ及びＰＭＯＳを得ることができ、リーク電流の増大を防止することができる。また、ＮＭＯＳの閾値を適正化することも可能である。

【００６１】本実施形態においても第１の実施形態と同様に、シリコン基板のｐ型ベース層３から絶縁層パターン１１上にかけてアモルファスシリコン層を形成し、このアモルファスシリコン層をシリコン基板を種結晶として単結晶化する。この単結晶化によって、絶縁層パターン１１上のアモルファスシリコン層も種結晶に近い部分が一部単結晶化する。この単結晶化したアモルファスシリコン層の部分にＮＭＯＳのチャネル領域３２の一部及びドレイン層３１ｂを形成することにより、ＮＭＯＳのリーク電流の増大を確実に防止することが可能である。特に、チャネル領域５２は種結晶となるシリコン基板に近いので、チャネル領域５２において良い結晶性を得ることが可能であり、リーク電流防止の効果は大きい。さらに、ＮＭＯＳのチャネル領域３２をアモルファスシリコン層の単結晶化領域に、ドレイン層３１ｂをその先の単結晶化しなかったポリシリコン領域に形成することも可能であり、この場合にもＮＭＯＳのリーク電流の増大を防止することができる。

【００６２】さらにまた、絶縁層パターン１１がシリコン基板とエピタキシャル単結晶シリコン層１２との間に介在するので、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層１、ｎ型ベース層２、ｐ型ベース層３、及びＮＭＯＳのn^+型のドレイン層３１ｂによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００６３】なお、第１の実施形態と同様にｐ型ベース層３の表面には当該ｐ型ベース層３よりも高濃度のp^+型拡散層が形成され、このp^+型拡散層の表面にチャネル領域３２、ソース層３１ａ、コンタクト層３１ｃが形成されるようにしても良い。これにより、第１の実施形態と同様に、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層１、ｎ型ベース層２、ｐ型ベース層３、及びＮＭＯＳのn^+型のソース層３１ａによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００６４】このように、本実施形態によれば、良好なＮＭＯＳ及びＰＭＯＳ特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でＩＧＢＴと一体的に構成することが可能である。

【００６５】（第３の実施形態）図３は、本発明の第３の実施形態に係わる高耐圧半導体装置を示す断面図である。図２と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第２の実施形態と異なる点は、絶縁層パターン上に形成されたエピタキシャル単結晶シリコン層の一部分に、ＮＭＯＳのドレイン層、チャネル領域の全部、及びソース層の一部が形成されている点である。

【００６６】図３に示すように、高耐圧半導体素子としてトレンチゲート型縦型ＩＧＢＴが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるＣＭＯＳ型半導体素子が形成されている。

【００６７】即ち、シリコン基板上には選択的に絶縁層パターン１１が形成され、この絶縁層パターン１１上に一部乗り上げるようにしてｐ型ベース層３上にエピタキシャル単結晶シリコン層１２が設けられている。また、絶縁層パターン１１上には多結晶（ポリ）シリコン層１２ｆが設けられている。エピタキシャル単結晶シリコン層１２にはＮＭＯＳが、絶縁層パターン１１上のポリシリコン層１２ｆにはＰＭＯＳ（図示せず）がそれぞれ形成されており、ＮＭＯＳとＰＭＯＳとは素子分離絶縁膜１２ｃによりお互いに分離されている。

【００６８】即ち、ＮＭＯＳは、エピタキシャル単結晶シリコン層１２に形成されたn^+型のソース層５１ａ及びドレイン層５１ｂ、これらの間に形成されたチャネル領域５２、この上にゲート絶縁層５３を介して形成されたゲート電極５４、ソース層５１ａに隣接して形成されたp^+型のコンタクト層５１ｃ、ソース層５１ａ及びコンタクト層５１ｃにコンタクトするソース電極５５ａ、ドレイン層５１ｂにコンタクトするドレイン電極５５ｂから構成されている。ＮＭＯＳのドレイン層５１ｂ、チャネル領域５２の全部分、及びソース層５１ａの一部分は絶縁層パターン１１上のエピタキシャル単結晶シリコン層１２の一部分に形成され、ソース層５１ａの一部分は絶縁層パターン１１が存在しないｐ型ベース層３表面のエピタキシャル単結晶シリコン層１２の一部分に形成されている。

【００６９】本実施形態によれば、第１の実施形態と同様にチャネル移動度及び飽和特性において良好なＮＭＯＳ及びＰＭＯＳを得ることができ、リーク電流の増大を防止することができる。また、ＮＭＯＳの閾値を適正化することも可能である。

【００７０】本実施形態においても第２の実施形態と同様に、シリコン基板のｐ型ベース層３から絶縁層パターン１１上にかけて形成したアモルファスシリコン層を、シリコン基板を種結晶として単結晶化する。この単結晶化によって、絶縁層パターン１１上のアモルファスシリコン層も種結晶に近い部分が一部単結晶化し、この単結晶化したアモルファスシリコン層の部分にＮＭＯＳのドレイン層５１ｂ、チャネル領域５２の全部分、及びソース層５１ａの一部分を形成することにより、ＮＭＯＳのリーク電流の増大を確実に防止することが可能である。特に、チャネル領域５２は種結晶となるシリコン基板に近いので、チャネル領域５２において良い結晶性を得る

ことが可能であり、リーク電流防止の効果は大きい。さらに、ＮＭＯＳのチャネル領域５２をアモルファスシリコン層の単結晶化領域に、ドレイン層５１ｂをその先の単結晶化しなかったポリシリコン領域に形成することも可能であり、この場合にもＮＭＯＳのリーク電流の増大を防止することができる。また、かかる構造ではＮＭＯＳのチャネル領域５２がシリコン基板から完全に絶縁されているので、かかるチャネル領域５２はシリコン基板の電位の影響を受け難く、しきい値の設定、制御が容易になる。

【００７１】さらにまた、絶縁層パターン１１により、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層１、ｎ型ベース層２、ｐ型ベース層３、及びＮＭＯＳのｎ$^+$型のドレイン層５１ｂによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００７２】なお、第１の実施形態と同様にｐ型ベース層３の表面には当該ｐ型ベース層３よりも高濃度のｐ$^+$型拡散層が形成され、このｐ$^+$型拡散層の表面にソース層５１ａ、コンタクト層５１ｃが形成されるようにしても良い。これにより、第１の実施形態と同様に、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層１、ｎ型ベース層２、ｐ型ベース層３、及びＮＭＯＳのｎ$^+$型のソース層５１ａによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００７３】このように、本実施形態によれば、良好なＮＭＯＳ及びＰＭＯＳ特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でＩＧＢＴと一体的に構成することが可能である。

【００７４】（第４の実施形態）図４は、本発明の第４の実施形態に係わる高耐圧半導体装置を示す断面図である。図１と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第１の実施形態と異なる点は、シリコン基板のＩＧＢＴのｐ型ベース層にＮＭＯＳが形成され、このＮＭＯＳとｐ型ベース層との間に高濃度のｐ型層が形成されている点である。

【００７５】図４に示すように、高耐圧半導体素子としてトレンチゲート型縦型ＩＧＢＴが半導体基板に形成されており、この高耐圧半導体素子と同一チップ上に以下に述べるＣＭＯＳ型半導体素子が形成されている。

【００７６】即ち、シリコン基板上には選択的に絶縁層パターン１１が形成され、この絶縁層パターン１１上には多結晶（ポリ）シリコン層１２ｇが設けられている。このポリシリコン層１２ｇにはＰＭＯＳが形成されている。また、ｐ型ベース層３中のＮＭＯＳが形成される領域には、ｐ型ベース層３よりも低濃度のｐ型半導体層３ｂが選択的に形成され、このｐ型半導体層３ｂにＮＭＯＳが形成されている。ＮＭＯＳとＰＭＯＳとは素子分離絶縁膜１２ｄによりお互いに分離されている。

【００７７】即ち、ＮＭＯＳは、ｐ型半導体層３ｂに形成されたｎ$^+$型のソース層６１ａ及びドレイン層６１ｂ、これらの間に形成されたチャネル領域６２、この上にゲート絶縁層６３を介して形成されたゲート電極６４、ソース層６１ａに隣接して形成されたｐ$^+$型のコンタクト層６１ｃ、ソース層６１ａ及びコンタクト層６１ｃにコンタクトするソース電極６５ａ、ドレイン層６１ｂにコンタクトするドレイン電極６５ｂから構成されている。上記ＮＭＯＳ下のｐ型半導体層３ｂには当該ｐ型半導体層３ｂ又はｐ型ベース層３よりも高濃度のｐ$^+$型拡散層３ｃが形成されている。

【００７８】一方、ＰＭＯＳは、ポリシリコン層１２ｇに形成されたｎ$^+$型のソース層７１ａ及びドレイン層７１ｂ、これらの間に形成されたチャネル領域７２、この上にゲート絶縁層７３を介して形成されたゲート電極７４、ソース層７１ａ及びドレイン層７１ｂにそれぞれコンタクトするソース電極７５ａ及びドレイン電極７５ｂから構成されている。

【００７９】本実施形態によれば、シリコン基板のｐ型半導体層３ｂにＮＭＯＳが形成されているので、結晶性の良い単結晶部分にＮＭＯＳが形成されていることになり、第１の実施形態と同様にチャネル移動度及び飽和特性において良好なＮＭＯＳ及びＰＭＯＳを得ることができ、リーク電流の増大を防止することができる。

【００８０】また、ＩＧＢＴのｐ型ベース層３よりも低濃度のｐ型半導体層３にＮＭＯＳが形成されているので、当該ＮＭＯＳの閾値を適正化することも可能である。このｐ型半導体層３の形成は、ＩＧＢＴのｐ型ベース層の形成に先立って行われる。

【００８１】さらにまた、ｐ型半導体層３ｂ又はｐ型ベース層３よりも高濃度のｐ$^+$型拡散層３ｃにより、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層１、ｎ型ベース層２、ｐ型ベース層３、及びＮＭＯＳのｎ$^+$型のソース層６１ａ又はドレイン層６１ｂによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００８２】このように、本実施形態によれば、良好なＮＭＯＳ及びＰＭＯＳ特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でＩＧＢＴと一体的に構成することが可能である。

【００８３】（第５の実施形態）図５は、本発明の第５の実施形態に係わる高耐圧半導体装置を示す断面図である。図４と同一部分には同一の符号を付して示し詳細な説明は省略する。本実施形態が第４の実施形態と異なる点は、絶縁層パターン上に形成された多結晶（ポリ）シリコン層にダイオードが形成されている点である。

【００８４】図５に示すように、高耐圧半導体素子としてトレンチゲート型縦型ＩＧＢＴが半導体基板に形成さ

れており、この高耐圧半導体素子と同一チップ上に以下に述べるダイオードが形成されている。

【００８５】即ち、シリコン基板上には選択的に絶縁層パターン１１が形成され、この絶縁層パターン１１上には多結晶（ポリ）シリコン層が設けられている。このポリシリコン層にはダイオードが形成されている。また、ｐ型ベース層３中のＮＭＯＳが形成される領域には、ｐ型ベース層３よりも低濃度のｐ型半導体層３ｂが選択的に形成され、このｐ型半導体層３ｂにＮＭＯＳが形成されている。ＮＭＯＳとダイオードとは素子分離絶縁膜１２ｅによりお互いに分離されている。

【００８６】即ち、ＮＭＯＳは、ｐ型半導体層３ｂに形成されたn^+型のソース層８１ａ及びドレイン層８１ｂ、これらの間に形成されたチャネル領域８２、この上にゲート絶縁層８３を介して形成されたゲート電極８４、ソース層８１ａに隣接して形成されたp^+型のコンタクト層８１ｃ、ソース層８１ａ及びコンタクト層８１ｃにコンタクトするソース電極８５ａ、ドレイン層８１ｂにコンタクトするドレイン電極８５ｂから構成されている。上記ＮＭＯＳ下のｐ型半導体層３ｂには当該ｐ型半導体層３ｂ又はｐ型ベース層３よりも高濃度のp^+型拡散層３ｃが形成されている。

【００８７】一方、ダイオードは、ポリシリコン層に形成されたp^+型のアノード層９１ａ、n^+型のカソード層９１ｂ、アノード層９１ａ及びカソード層９１ｂにそれぞれコンタクトするアノード電極９２ａ及びカソード電極９２ｂから構成されている。

【００８８】本実施形態によれば、第４の実施形態と同様にチャネル移動度及び飽和特性において良好なＮＭＯＳを得ることができ、リーク電流の増大を防止することができる。

【００８９】また、第４の実施形態と同様にｐ型半導体層３によりＮＭＯＳの閾値を適正化することも可能である。さらに、p^+型拡散層３ｃにより、シリコン基板に設けたＩＧＢＴのｐ型ドレイン層１、ｎ型ベース層２、ｐ型ベース層３、及びＮＭＯＳのn^+型のソース層８１ａ又はドレイン層８１ｂによって寄生サイリスタが構成されることを防止でき、素子のサイリスタ動作を抑制することが可能である。

【００９０】このように、本実施形態によれば、良好なＮＭＯＳ特性を得ることができるため、ドライブ回路や保護回路等のアナログ、デジタル各種回路を高精度でＩＧＢＴと一体的に構成することが可能である。

【００９１】なお、本発明は上記実施形態に限定されるものではない。例えば、p^+型ドレイン層１とｎ型ベース層２との間には当該ｎ型ベース層２よりも高濃度のｎ型バッファ層を形成することができ、導電率を向上させることが可能である。

【００９２】また、上記実施形態では縦型の高耐圧半導体装置について説明したが、本発明は横型の高耐圧半導体装置に対しても適用可能である。この場合、ドレイン層はソース層と同じ側の半導体基板表面に形成する。

【００９３】さらにまた、上記実施形態ではp^+型のドレイン層を有するＩＧＢＴを例に挙げて説明したが、ドレイン層をn^+型としてＭＯＳ型高耐圧半導体素子、その他サイリスタ等、各種高耐圧半導体素子に対して適用することも可能である。その他、本発明の趣旨を逸脱しない範囲で種々変形して実施することが可能である。

【００９４】

【発明の効果】本発明によれば、高耐圧素子及びドライブ回路や保護回路等を一体化した高耐圧半導体装置を信頼性高く低コストで提供することができる。

【図面の簡単な説明】

【図１】　本発明の第１の実施形態に係わる高耐圧半導体装置を示す断面図。

【図２】　本発明の第２の実施形態に係わる高耐圧半導体装置を示す断面図。

【図３】　本発明の第３の実施形態に係わる高耐圧半導体装置を示す断面図。

【図４】　本発明の第４の実施形態に係わる高耐圧半導体装置を示す断面図。

【図５】　本発明の第５の実施形態に係わる高耐圧半導体装置を示す断面図。

【図６】　従来の高耐圧半導体装置を示す断面図。

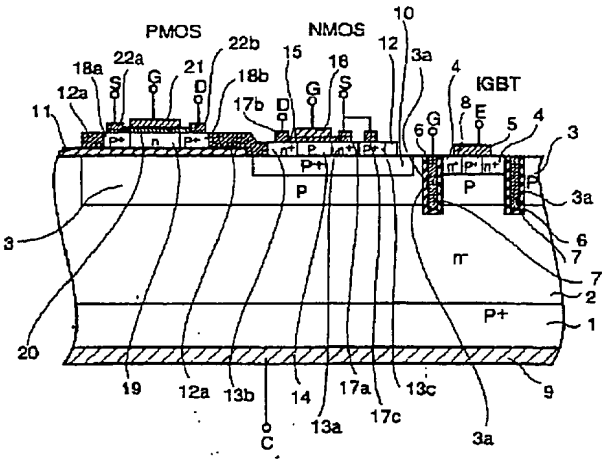
【図７】　ＮＭＯＳ及びＰＭＯＳの電圧と電流との関係を示した特性図。

【符号の説明】

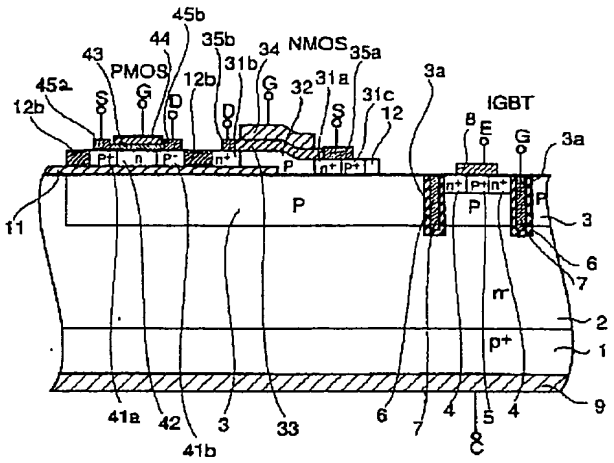
１　p^+型ドレイン層
２　ｎ型ベース層
３　ｐ型ベース層
３ａ　トレンチ
４　n^+型ソース層
５　p^+型コンタクト層
６　ゲート絶縁膜
７　ゲート電極
８　ソース電極
９　ドレイン電極
１０　p^+型拡散層
１１　絶縁層パターン
１２　エピタキシャル単結晶シリコン層
１２ａ　素子分離絶縁膜
１３ａ　n^+型のソース層
１３ｂ　n^+型のドレイン層
１３ｃ　コンタクト層
１４　チャネル領域
１５　ゲート絶縁層
１６　ゲート電極
１７ａ　ソース電極
１７ｂ　ドレイン電極
１７ｃ　コンタクト電極

１８ａ　n⁺ 型のソース層
１８ｂ　ドレイン層
１９　チャネル領域
２０　ゲート絶縁層
２１　ゲート電極
２２ａ　ソース電極
２２ｂ　ドレイン電極

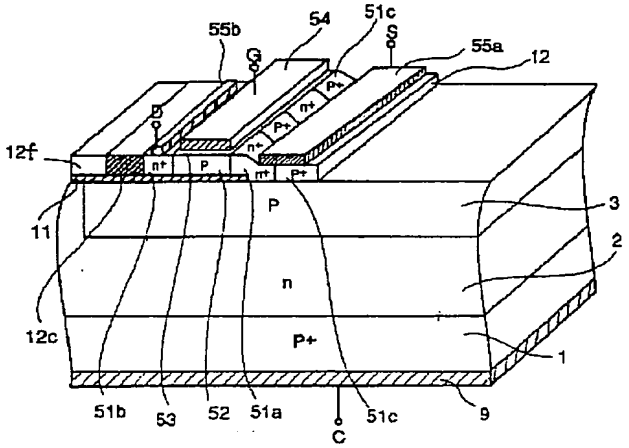
【図１】



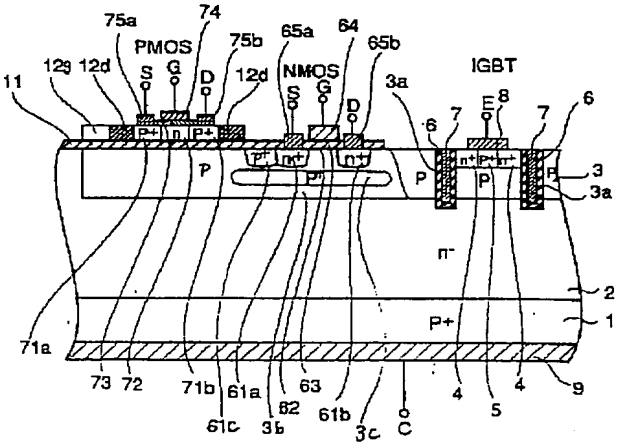
【図２】



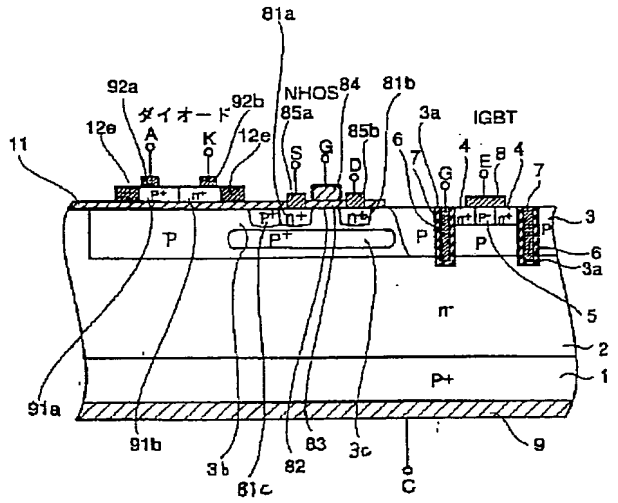
【図３】



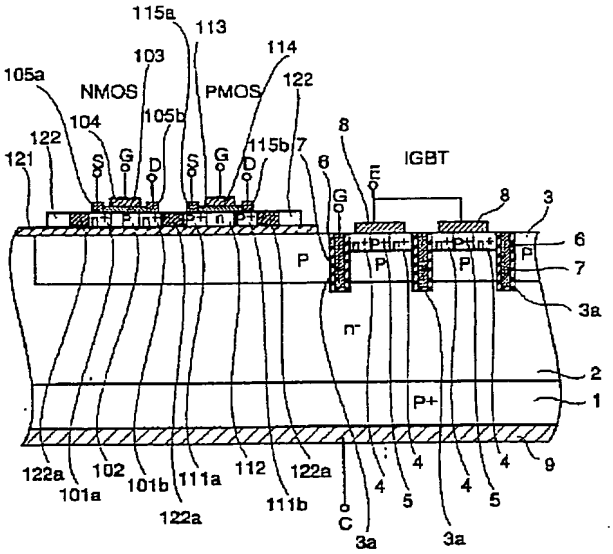
【図４】



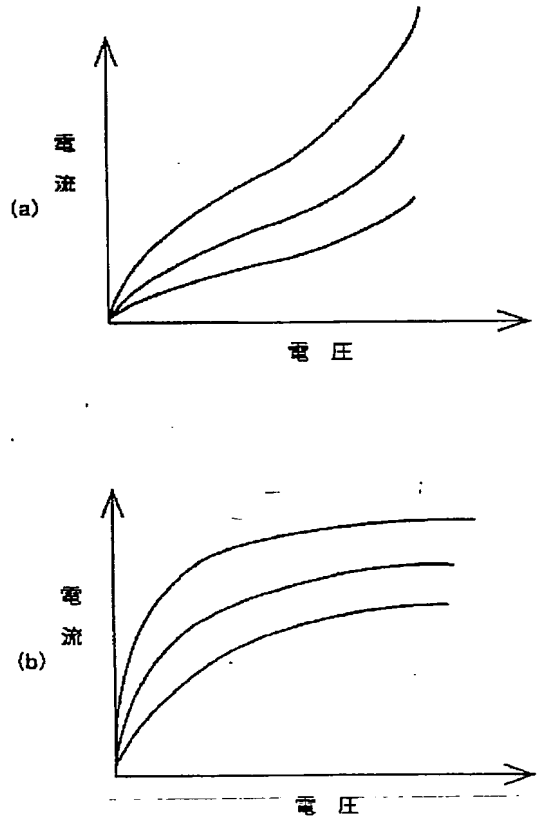
【図５】


81a
92a
ダイオード
92b
NHOS
84
81b
12e
A
K
12e
85a
85b
3a
IGBT
11
S
G
D
6
7
G
4
E
8
4
7
3
6
3a
5
2
1
91a
91b
3b
81c
82
83
3c
C
9

【図６】


115a
113
103
114
105a
NMOS
PMOS
122
104
105b
122
121
S
G
D
S
G
D
115b
7
8
6
G
IGBT
8
3
6
7
3a
2
1
122a
101a
102
101b
111a
122a
112
111b
122a
C
3a
4
5
4
5
3a
9

【図７】


(a)
電流
電圧
(b)
電流
電圧

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(51)Int.Cl.[7]	識別記号	F I		テーマコード（参考）
Ｈ０１Ｌ 27/092		Ｈ０１Ｌ 29/78	６１３Ａ	
29/78			６５３Ａ	
29/786			６５５Ａ	
			６５６Ｄ	
			６５７Ｃ	

Ｆターム(参考) 5F038 BH04 BH12 EZ14 EZ20
5F040 DA00 DA06 DA23 DB01 DB03
DB06 DC01 EB12 EB14 EC19
EM00 EM01 EM03 EM04 FC07
5F048 AA03 AA07 AC01 AC03 AC10
BA02 BA12 BA20 BB01 BB05
BC11 BC16 BC18 BC19 BD09
BE08 BG06 BH01 CB07 CC04
CC06 CC15 CC16 CC18
5F110 AA06 AA08 BB04 CC02 DD05
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PP01 PP10